

Compiler-based Extraction of Event Arrival Functions for Real-Time Systems Analysis

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30th Euromicro Conference on Real-Time Systems (ECRTS), 2018





















Evaluation





Evaluation



















 Δt in Cycles





 Δt in Cycles





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Conclusion

Extracting Curves?

• Capture traces

 \Rightarrow Potentially unsafe

- Rely on specifications
 - \Rightarrow Potentially overly pessimistic
- Extraction based on the low-level representation



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• Explicit path analysis quickly becomes practically infeasible

 \Rightarrow Sliding window for all traces

 \Rightarrow Adapt path analysis techniques

 \Rightarrow Introduce granularity

• Trade-off between precision and runtime



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Path Analysis for Arrival Functions

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Event Arrival Functions

• Abstract notion of interfering events (e.g., task activations, shared memory accesses, ...)

Definition

Let $\eta_i^+(\Delta t)$ and $\eta_i^-(\Delta t)$ denote for each task *i* the maximum and minimum number of events issued within a time window of size Δt . Their pseudo-inverse counterparts $\delta^+(n)$ and $\delta^-(n)$, return the maximum/minimum time interval between the first and the last event in any sequence of *n* event arrivals.



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- Describe all feasible paths by formulating an Integer Linear Program (ILP) [DAC95]
- Enforcing complete path through a program using junction rules





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Adapted IPET

• First introduced by Jacobs et al. [RTNS15]

- Introduce "movable" sources and sinks
- Determine max. (resp. min.) number of events per basic block
- Maximize (resp. minimize) accumulated number of events over sub-path
 - \Rightarrow While accumulated time $w \leq \Delta t$ (resp. $w \geq \Delta t$)



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Automated Extraction

• Two dimensions of granularity:

- Events per basic block
- Sample rate
- Adjustable trade-off between runtime and tightness
 - Albeit, arrival functions will be safe

add ldr sub	r0, r6 , r6,	r1, #5 [r0] r6, #7	
ldr	r3,	[r9]	Ζ
orr str bne	: r1, r1 , Y	r0, r2 [r0]	

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add 1dr sub 1dr	r0, r6, r6, r 3,	r1, #5 [r0] r6, #7 [r9]	Z
orr str bne	r1, r1, r1, Y	r0, r2 [r0]	

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Overapproximation Metric

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Overapproximation Metric

Evaluation Setup

- MRTC benchmark suite
 - duff benchmark excluded (due to timing analysis tool incompatibility)
- Evaluations performed on an Intel Xeon Server (20 cores at 2.3 GHz, 94 GB RAM)
- ILPs solved using Gurobi 7.5.0
- Compiled with the WCET-aware C compiler (WCC) using the -02 flag
- ARM7TDMI architecture (without caches)
- Data object access triggers an event

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- Automated upper and lower event arrival function extraction from code-level analysis
- Two adjustable levels of granularity

- Adding calling contexts
- Optimizations based on the extracted functions



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