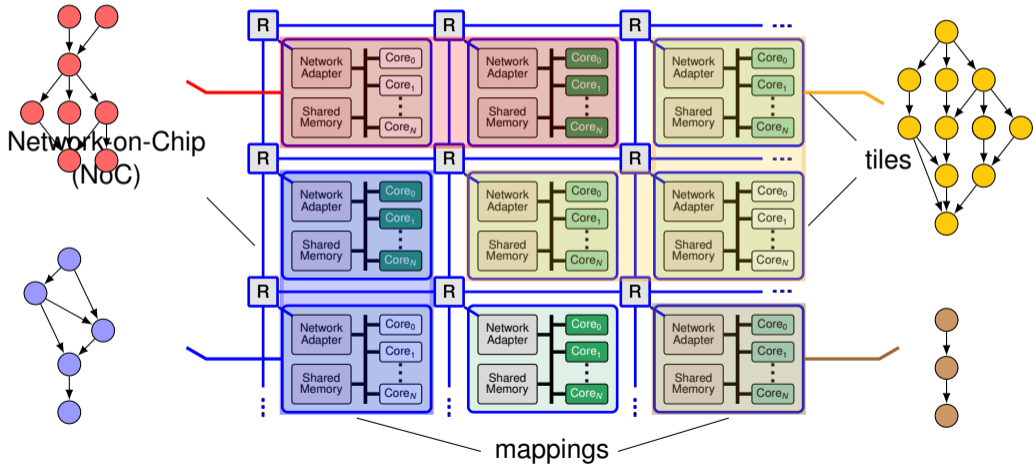# Isolation-Aware Timing Analysis and Design Space Exploration for Predictable and Composable Many-Core Systems

Behnaz Pourmohseni, Fedor Smirnov, Stefan Wildermann, and Jürgen Teich
Friedrich-Alexander University Erlangen-Nürnberg (FAU)
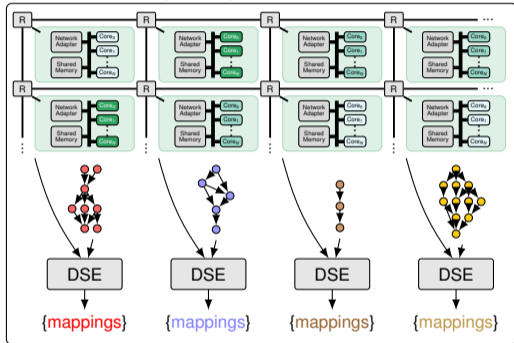July 11, 2019

Many-Core Systems: Overview

Network-on-Chip (NoC)

tiles

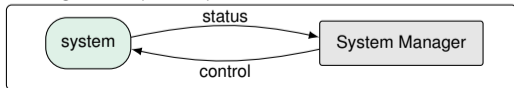mappings

Hybrid Application Mapping

$\rightarrow$ for real-time applications

- off-line timing verification

- composable systems

- *inter-application isolation*
  - spatial isolation
  - temporal isolation
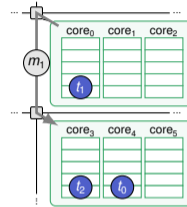   - TDM
    - WRR
    - …

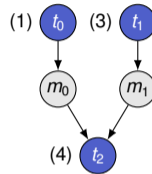- *customized timing analysis*

characterization (off-line)
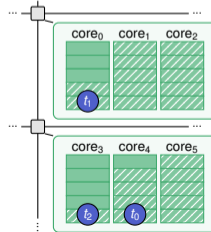
DSE DSE DSE DSE

{mappings} {mappings} {mappings} {mappings}

management (on-line)

system —status→ System Manager
system ←control— System Manager
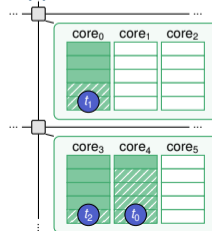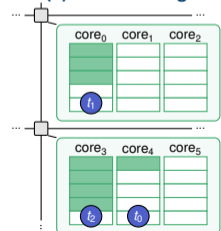
Inter-Application Isolation Schemes

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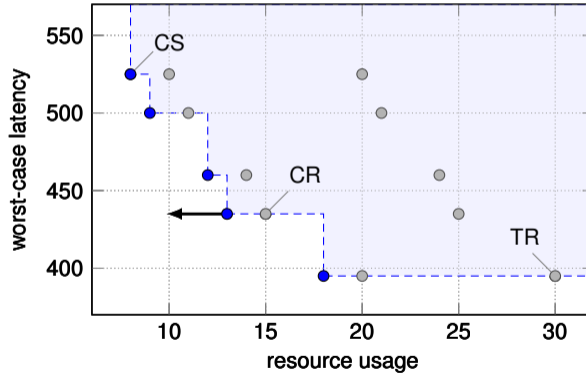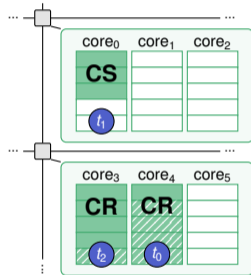
Isolation-Aware DSE: Contribution

- isolation-scheme exploration
- isolation-aware timing analysis

specification

mapping optimizer

binding, isolation,
routing, allocation, scheduling

Pareto-optimal mappings

mapping

quality numbers

evaluators

latency, resource cost,
energy, throughput, ...
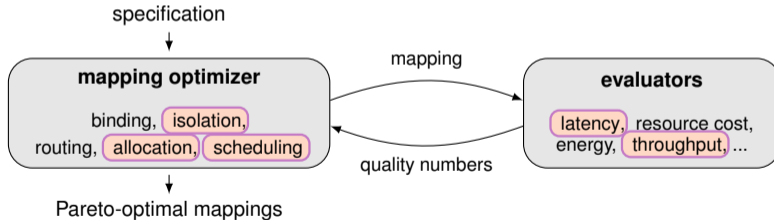
Isolation-Aware Exploration
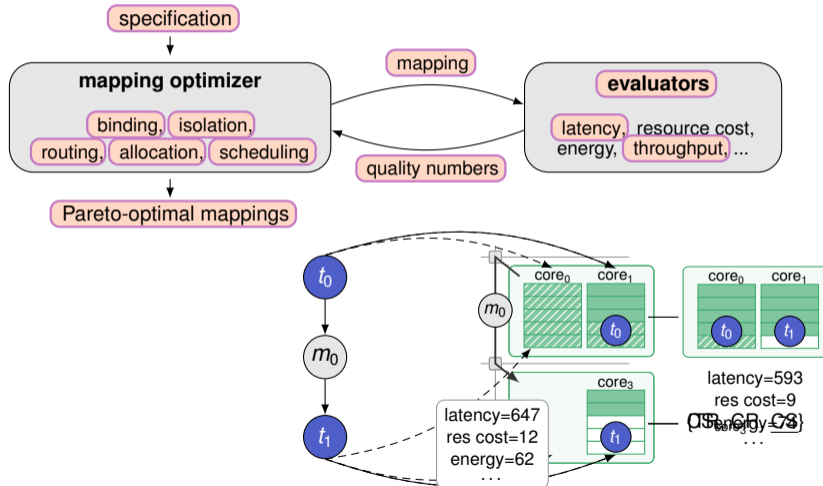
Worst-Case Timing Analysis

- task model
  - periodic, preemptive

- resource arbitration/scheduling
  - predictable & composable
  - time-triggered time slicing
  - work conserving

- timing analysis
  - response time (tasks)
  - traversal time (messages)

- **isolation awareness**
  - *arbitration tuple* (S, W, P)
    - per *requestor ▷ resource*
    - depends on optimizer's decisions

Arbitration Tuple (S, W, P)

$S = 5$ $D = 1$

$W_{t_1} = 1$ $W_{t_0} = 3$

shared with other apps

$(5, 1, 36)$ $(5, 3, 36)$

$P = 6 \times (S + D) = 36$

exclusive allocation

$(5, 1, 24)$ $(5, 3, 24)$

$P = 4 \times (S + D) = 24$
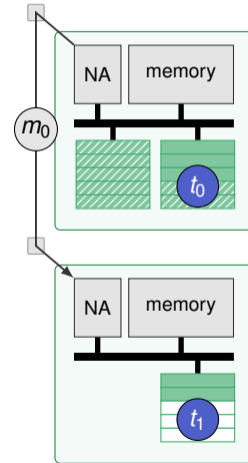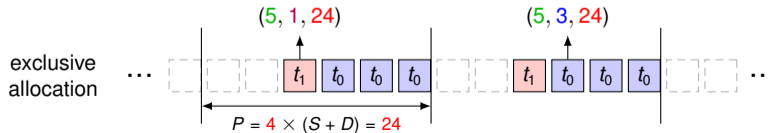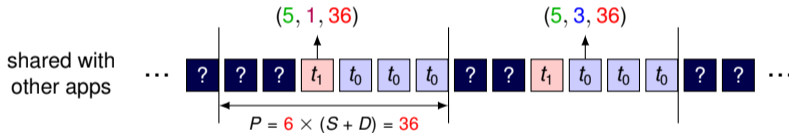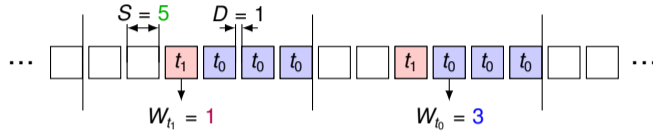
Arbitration Tuple (**S**, **W**, **P**)

- task ▷ core

- core ▷ bus

- NA (TX/RX) ▷ bus

- Message ▷ NA (TX)

- Message ▷ NoC

- Message ▷ NA (RX)

message ▷ NA (TX)
$(S_{tx_0}, W_{tx_0}^{m_0}, P_{tx_0}^{m_0})$

message ▷ NoC
$(\tau^{noc}, W_{\rho_{m_0}}^{m_0}, P_{\rho_{m_0}}^{m_0})$

message ▷ NA (RX)
$(S_{rx_1}, W_{rx_1}^{m_0}, P_{rx_1}^{m_0})$

NA (TX) ▷ bus
$(S_{b_0}, W_{b_0}^{tx_0}, P_{b_0}^{tx_0})$

core ▷ bus
$(S_{b_0}, W_{b_0}^{c_1}, P_{b_0}^{c_1})$

task ▷ core
$(S_{c_1}, W_{c_1}^{t_0}, P_{c_1}^{t_0})$

core ▷ bus
$(S_{b_1}, W_{b_1}^{c_3}, P_{b_1}^{c_3})$

task ▷ core
$(S_{c_3}, W_{c_3}^{t_1}, P_{c_3}^{t_1})$

NA (RX) ▷ bus
$(S_{b_1}, W_{b_1}^{rx_1}, P_{b_1}^{rx_1})$
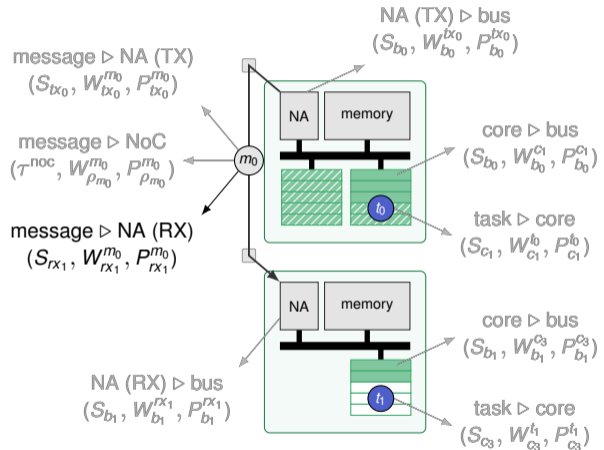
Response-Time Analysis

$$\text{WCRT}(t, c, q, b) = \underbrace{\text{WCET}(t, c)}_{\text{WCET}} + \underbrace{\text{MD}(t) \cdot \text{ST}(q, b)}_{\text{memory delay}} + \underbrace{I^{\text{bus}}(t, c, q, b)}_{\text{bus delay}} + \underbrace{I^{\text{core}}(t, c, q, b)}_{\text{preemption delay}}$$

$$I^{\text{bus}}(t, c, q, b) = \min\left\{\text{MD}(t), \left\lceil \frac{\text{WCET}(t, c) + \text{MD}(t) \cdot \text{ST}(q, b)}{S_b} \right\rceil\right\} \cdot \left(P_b^c - W_b^c \cdot S_b\right)$$

$$I^{\text{core}}(t, c, q, b) = \left\lceil \frac{\text{WCET}(t, c) + \text{MD}(t) \cdot \text{ST}(q) + I^{\text{bus}}(t, c, q, b)}{W_c^t \cdot S_c} \right\rceil \cdot \left(P_c^t - W_c^t \cdot S_c\right)$$

task ▷ core
(S_c, W_c^t, P_c^t)

core ▷ bus
(S_b, W_b^c, P_b^c)
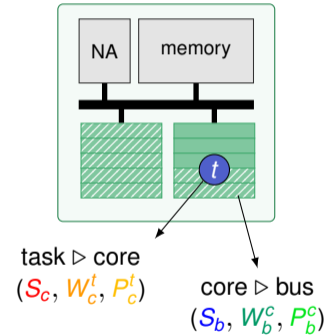
Traversal-Time Analysis

TX delay   NoC delay   RX delay

$$\text{WCTT}(m, tx, q, b, \rho, rx, \hat{q}, \hat{b}) = D^{\text{tx}}(m, tx, q, b) + D^{\text{noc}}(m, \rho) + D^{\text{rx}}(m, rx, \hat{q}, \hat{b})$$

$$
\begin{aligned}
D^{\text{tx}}(m, tx, q, b) = {} & \text{MD}(m) \cdot \text{ST}(q, b) \\
& + \left\lceil \left\lceil \text{MD}(m) \cdot \left\lceil \frac{S_b}{\text{ST}(q, b)} \right\rceil^{-1} \right\rceil \cdot \frac{1}{W_b^{tx}} \right\rceil \cdot \left(P_b^{tx} - W_b^{tx} \cdot S_b \right) \\
& + \left\lceil \left\lceil \left\lceil \text{MD}(m) \cdot \left\lceil \frac{S_b}{\text{ST}(q, b)} \right\rceil^{-1} \right\rceil \cdot \frac{1}{W_b^{tx}} \right\rceil \cdot \frac{1}{W_{tx}^m} \right\rceil \cdot \left(P_{tx}^m - W_{tx}^m \cdot S_{tx} \right)
\end{aligned}
$$

$$
D^{\text{noc}}(m, \rho) = \left(f_m - 1 + |\rho| \cdot D^{\text{router}} \right) \cdot \tau^{\text{noc}} + \left(\left\lceil \frac{f_m}{W_\rho^m} \right\rceil - 1 + |\rho| \right) \cdot \left(P_\rho^m - W_\rho^m \cdot \tau^{\text{noc}} \right)
$$

message ▷ NA (TX)
$(S_{tx}, W_{tx}^m, P_{tx}^m)$

NA (TX) ▷ bus
$(S_b, W_b^{tx}, P_b^{tx})$

message ▷ NoC
$(\tau^{\text{noc}}, W_\rho^m, P_\rho^m)$

NA   memory

m

NA   memory

message ▷ NA (RX)
$(S_{rx}, W_{rx}^m, P_{rx}^m)$

NA (RX) ▷ bus
$(S_{\hat{b}}, W_{\hat{b}}^{rx}, P_{\hat{b}}^{rx})$
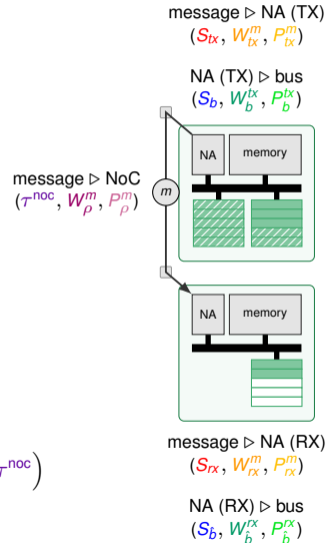
Experimental Results

Experimental Setup

platform architectures
- 4×4: 64 cores
- 5×5: 100 cores
- 6×6: 144 cores

applications
- networking (7 tasks)
- consumer (11 tasks)
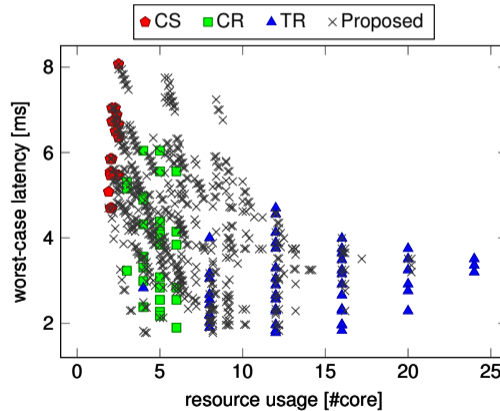- telecom. (14 tasks)
- automotive (18 tasks)

design objectives
- worst-case latency
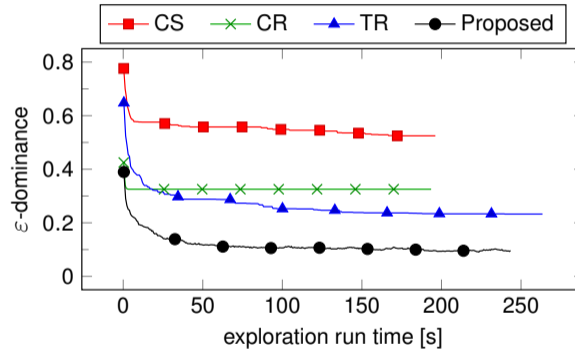- resource usage
- energy consumption

compared approaches
- tile reservation (TR)
- core reservation (CR)
- core sharing (CS)
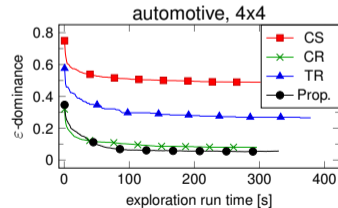- isolation aware (Proposed)

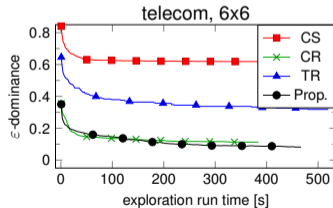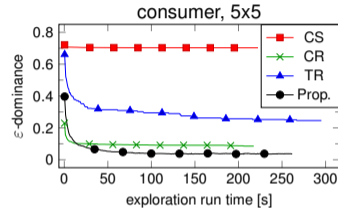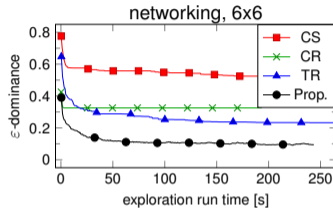# Results: Solution Distribution

Results: Optimization Performance

mapping quality $\uparrow \Rightarrow \varepsilon$-dominance $\downarrow$

Results: Optimization Performance (cont'd)

networking, 6x6 — consumer, 5x5 — telecom, 6x6 — automotive, 4x4

quality improvement → **26**% on average, up to **67**%

Conclusion

- inter-application isolation schemes *in combination*
    - extends the solution space
    - enables solutions of higher quality
- isolation-aware application mapping realized through
    - isolation-aware DSE
    - isolation-aware timing analysis
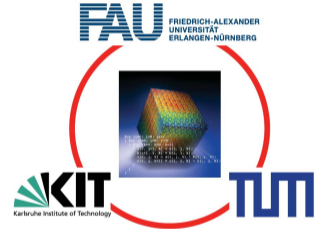
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