Experiments for Time-Predictable Execution of GPU Kernels

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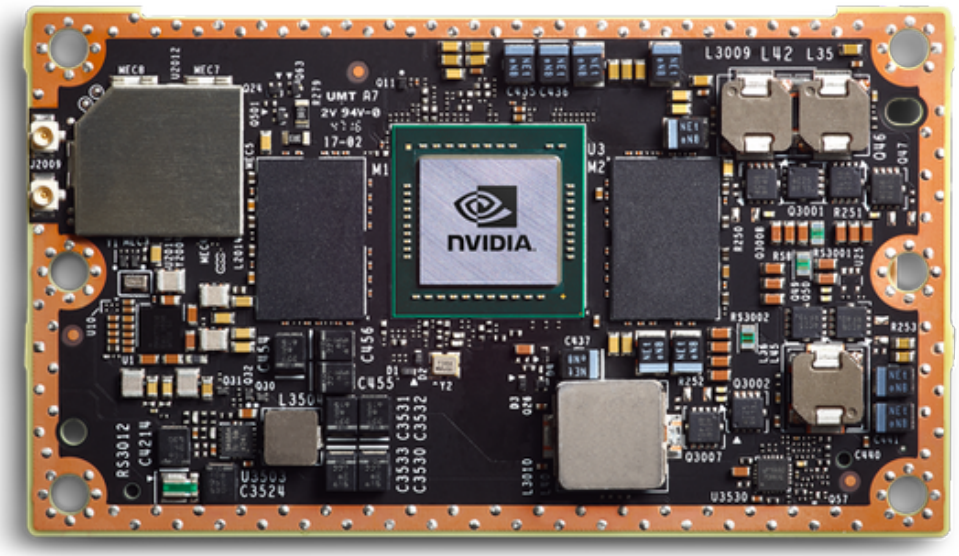
OSPERT 2019
July 9, 2019,
Stuttgart, Germany

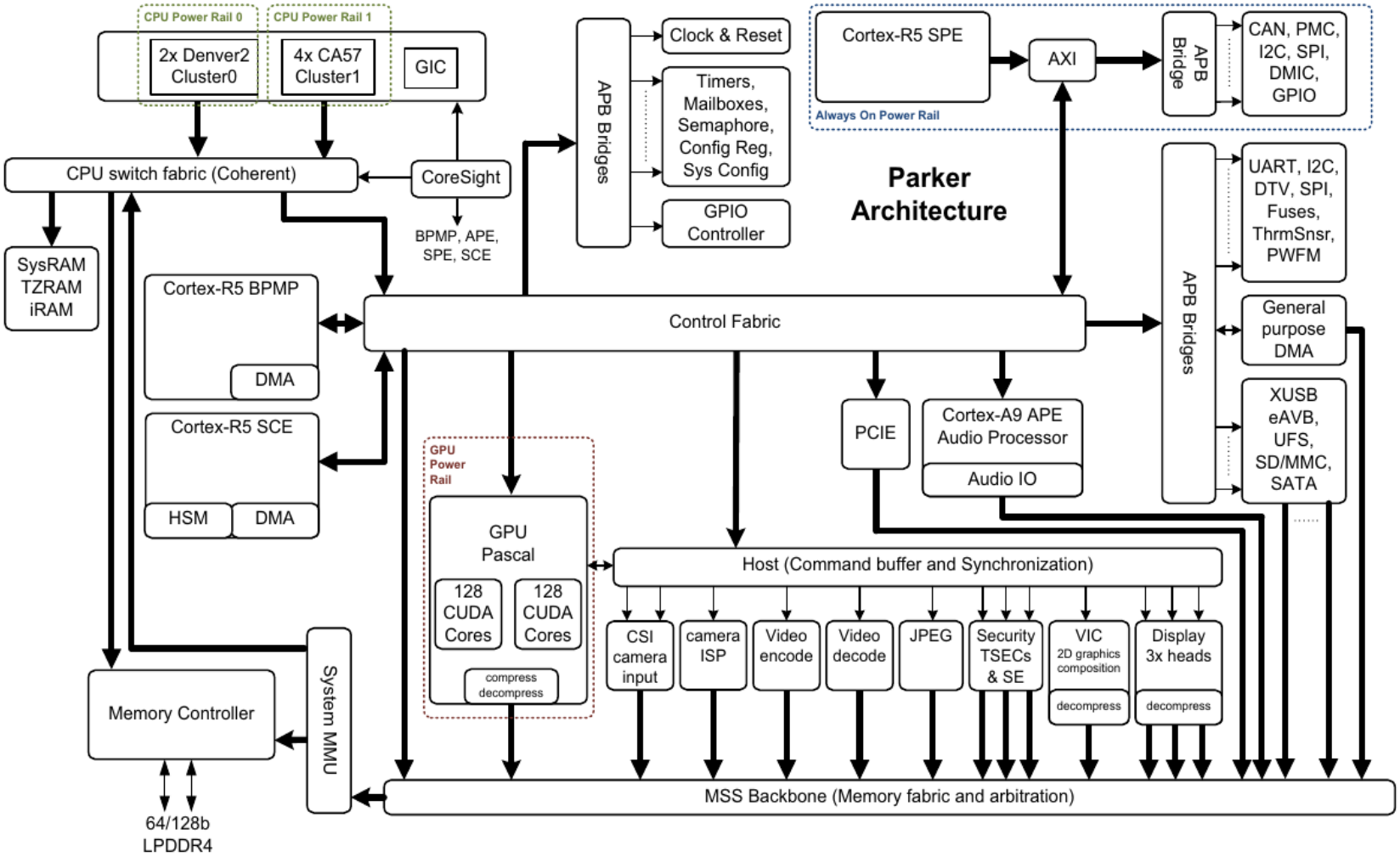
NVIDIA Tegra X2



- CPUs: 4× ARM Cortex A57, 2× Denver (ARM/NVIDIA)
- GPU: 256 CUDA cores in 2 streaming multiprocessors (SM)

Outline

NVIDIA Tegra X2 block diagram



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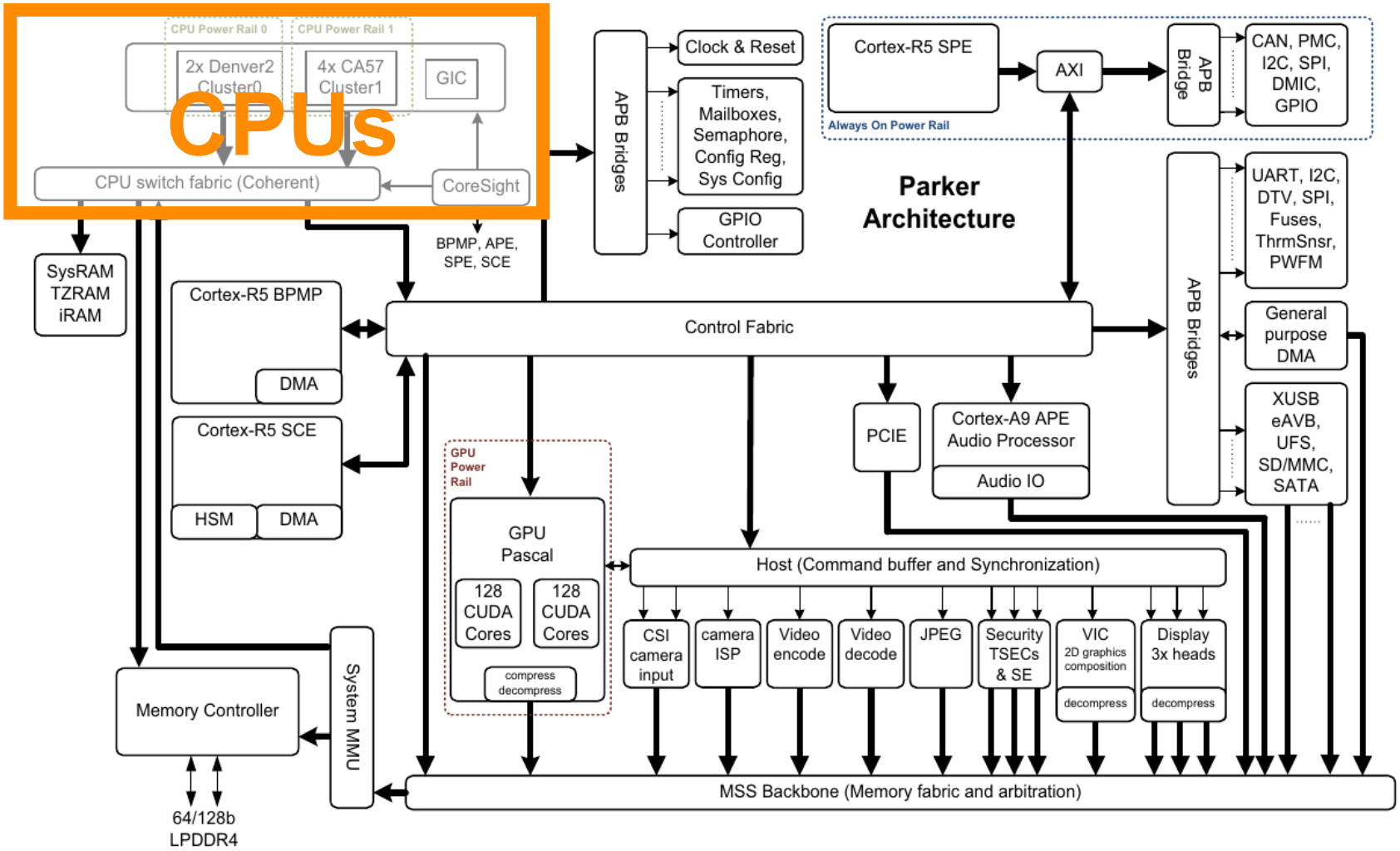

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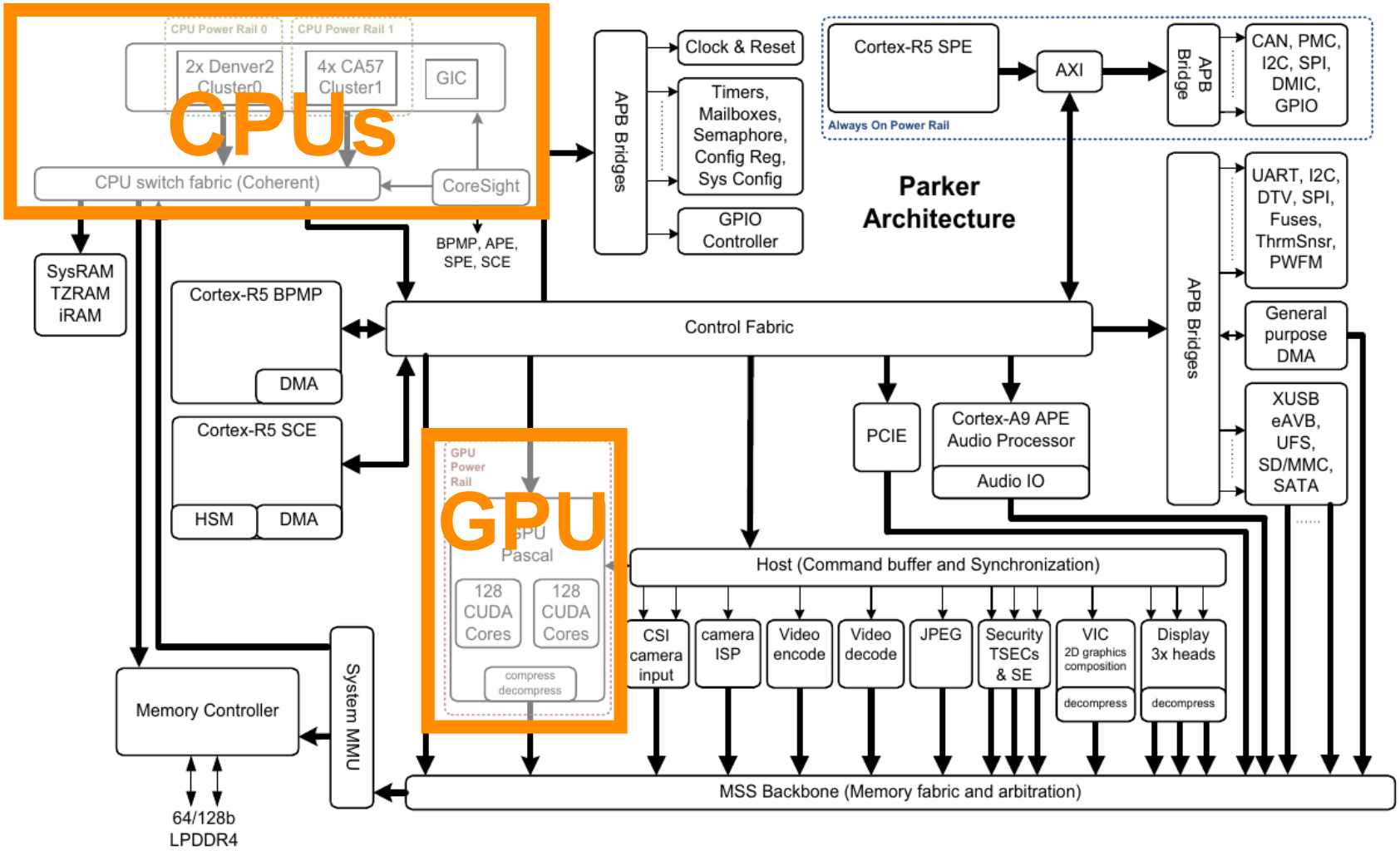

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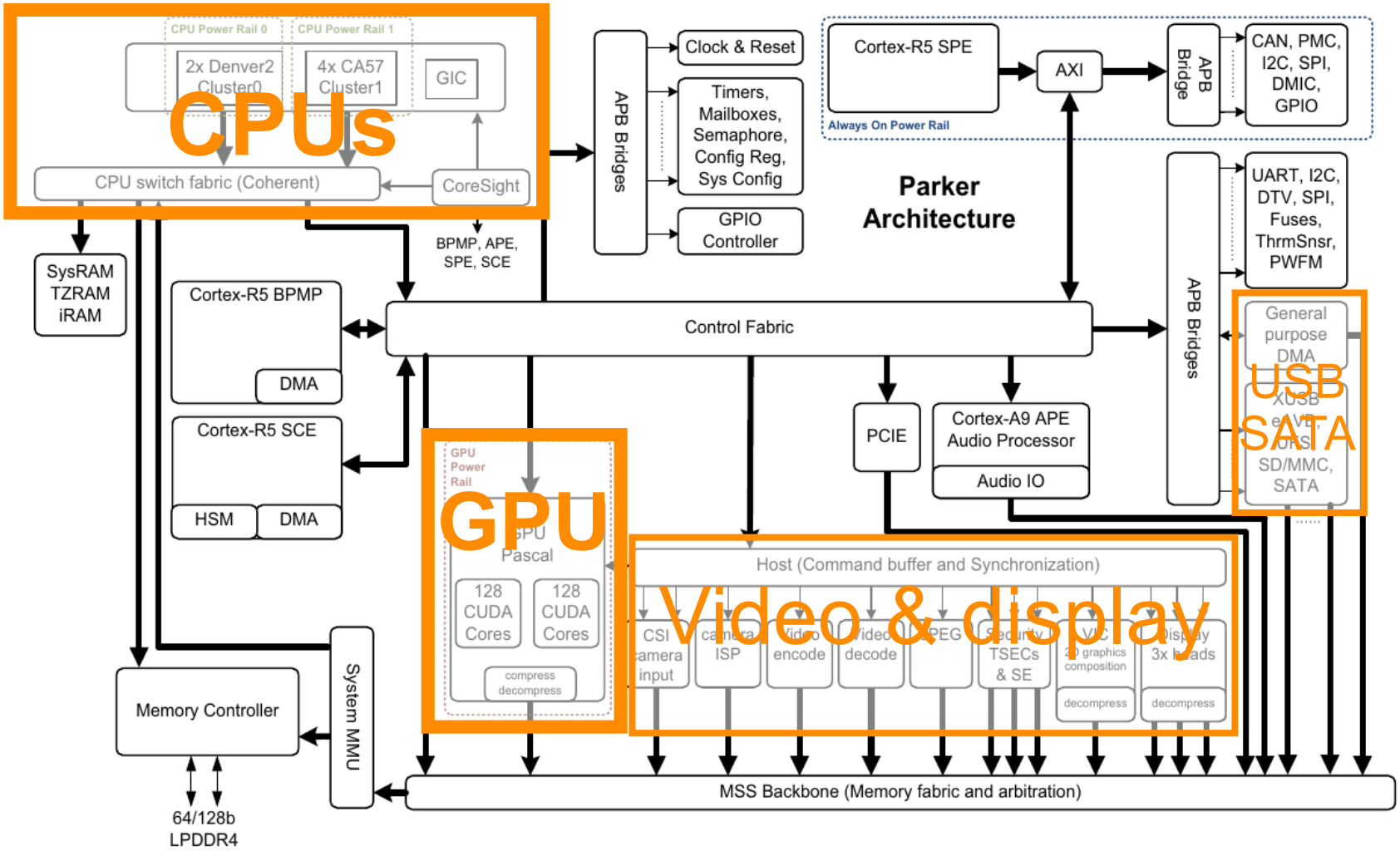

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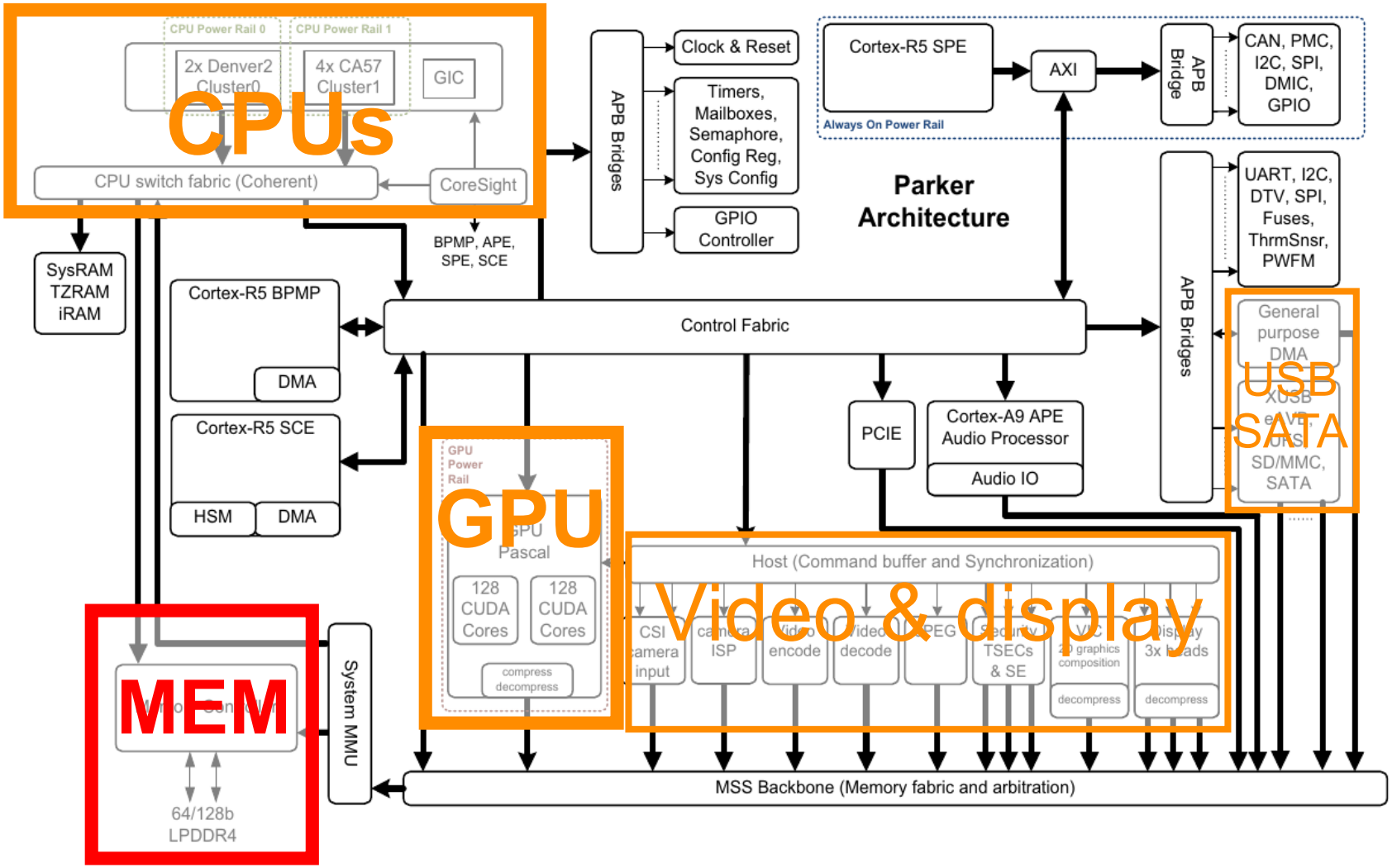
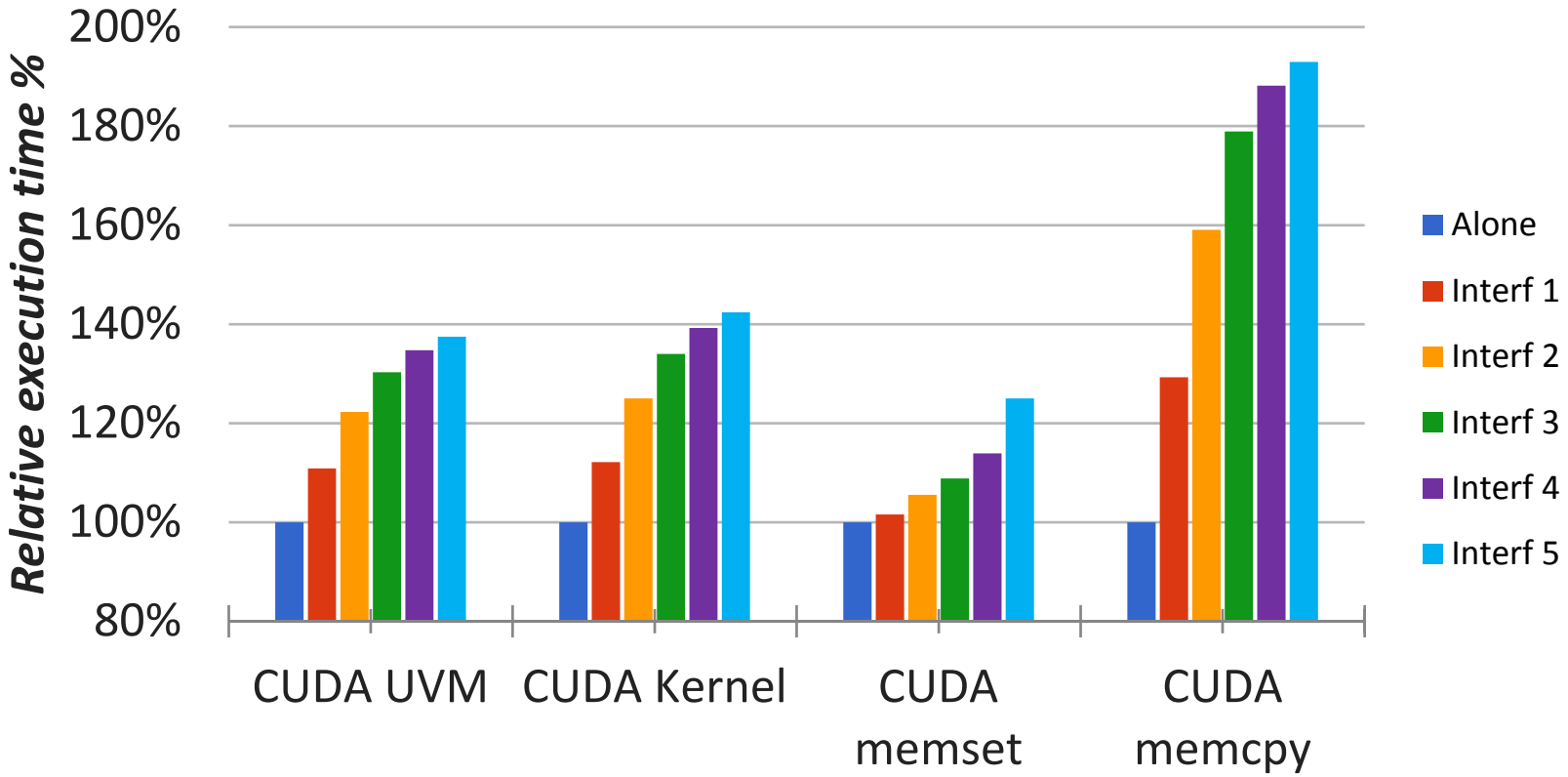


GPU execution times under CPU interference

Tegra X2, CPUs performing sequential memory accesses



Source: Capodieci et al., *Detailed characterization of platforms*, Deliverable D2.2, H2020 project HERCULES, 2017.

Safety-Critical applications

E.g. autonomous driving

- Future application will need to combine safety and high performance
- Typically, only some parts of the system are safety-critical
- **Goal:** isolate critical parts from non-critical ones
  - Failure in non-critical component should not propagate to a critical one

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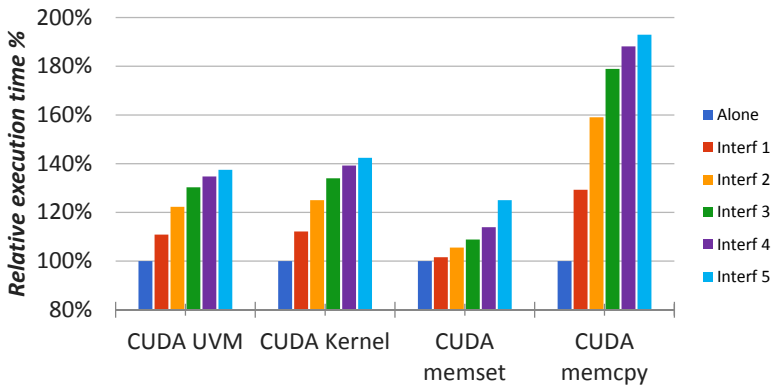
- ISO26262: **Freedom from interference**

Interference on TX2

1. CPU-to-GPU



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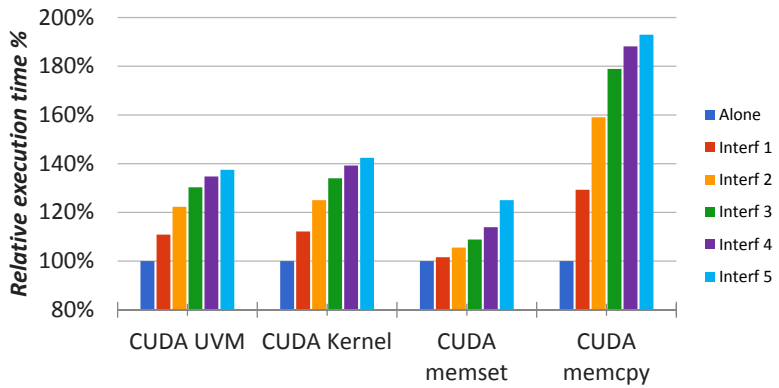

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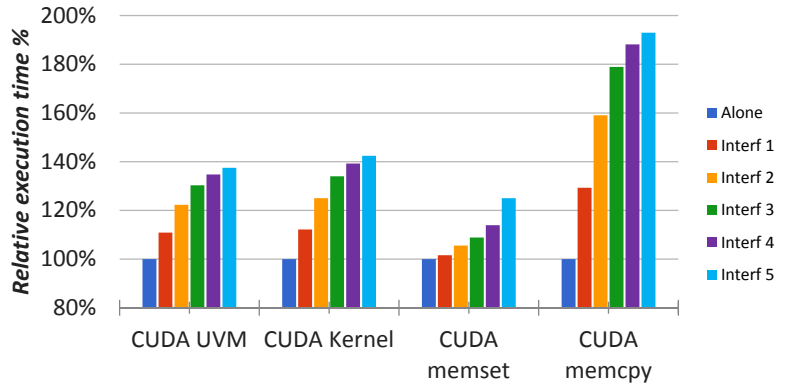

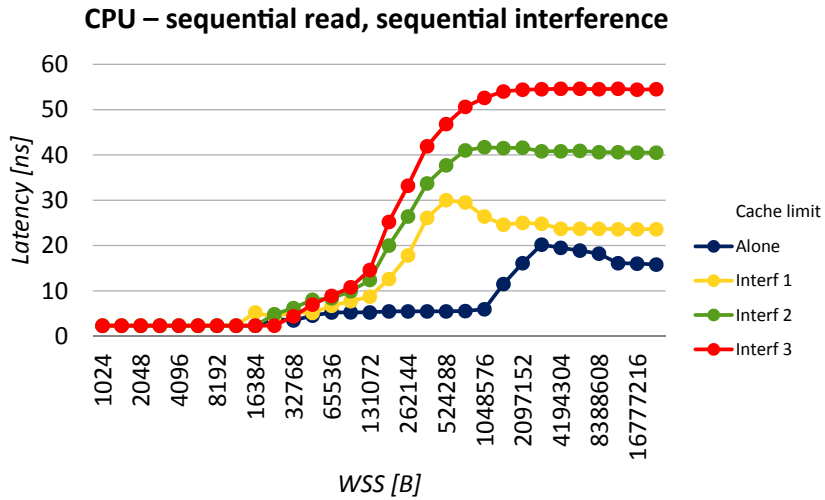

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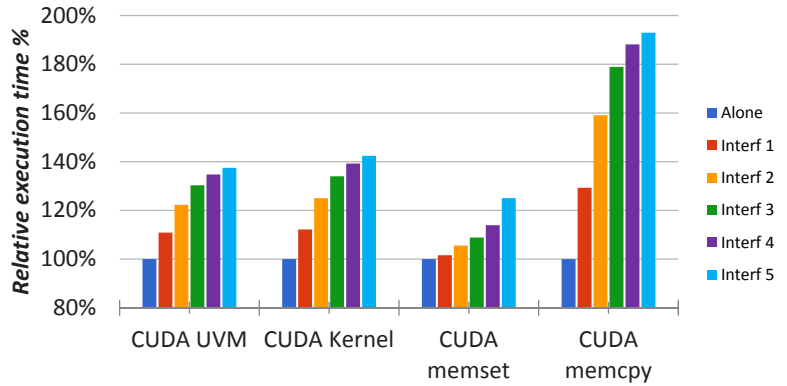

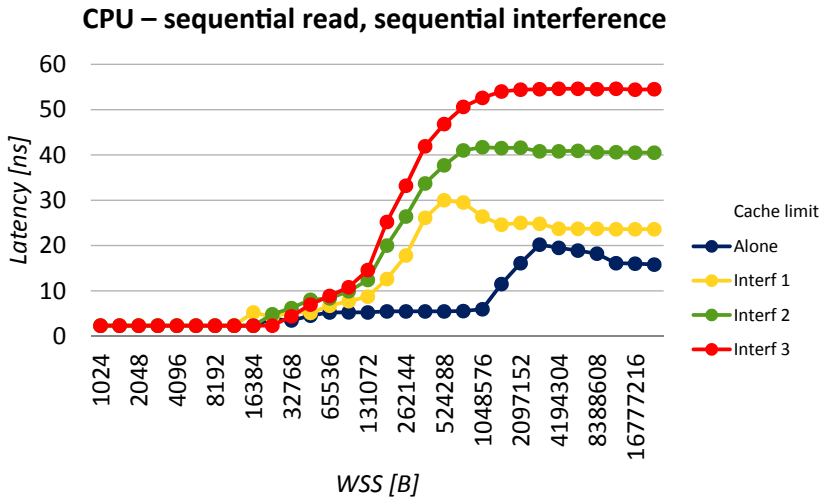

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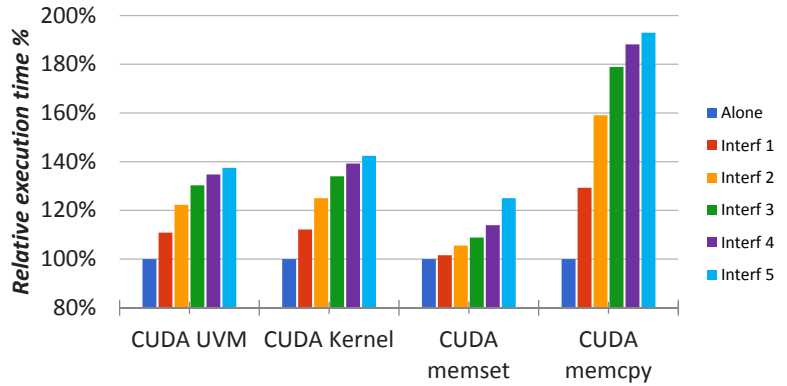

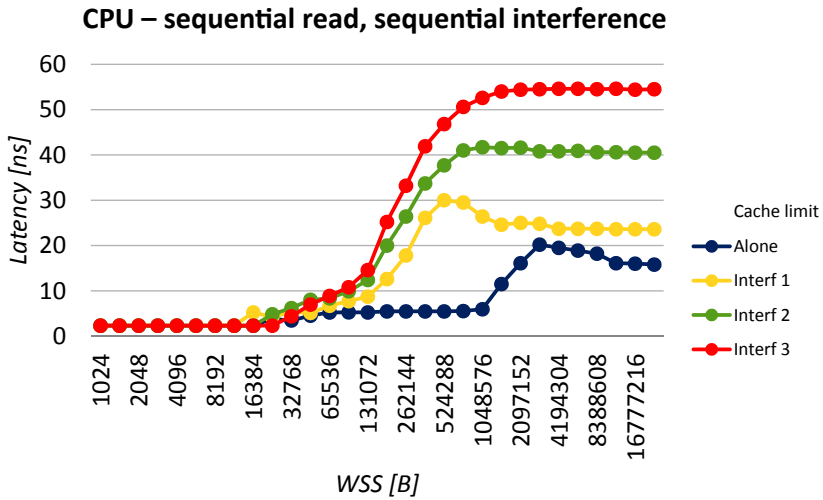

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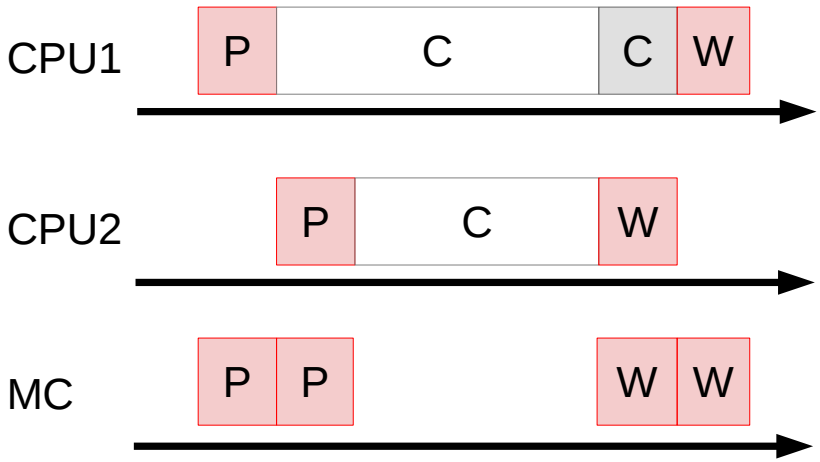
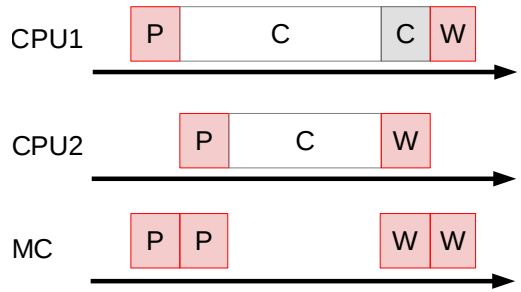
CPU-to-CPU interference

- Possible solution (a part of): **PRedictable Execution Model** (PREM)
- Tasks prefetch batches of data to CPU-local memory (cache/scratchpad) and synchronize on access to main memory
- Well applicable to number-crunching applications:
  - Image processing
  - Neural networks
- GPUs are better suited for these

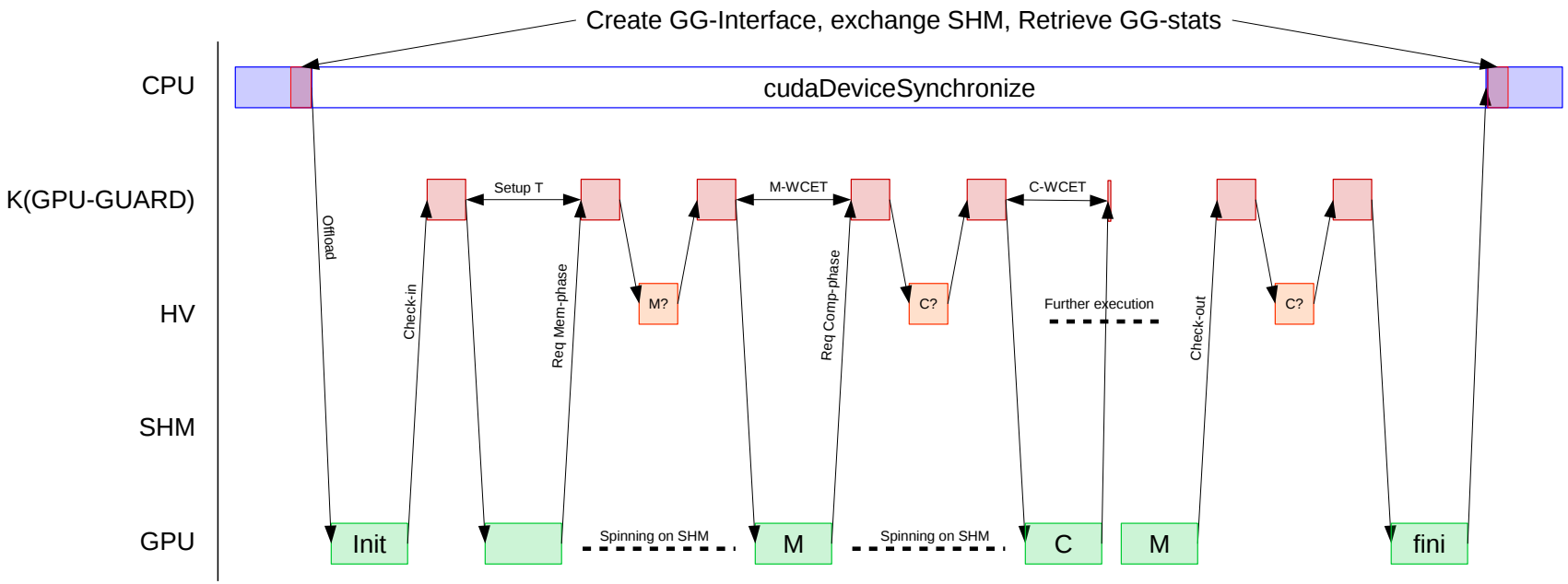


Problems with PREM on GPUs

- Memory bandwidth is almost always a bottleneck
- Compute-phases are shorter due to high parallelism
- Mutual exclusion for memory access kills performance
- Costly synchronization ($\approx 2\,\mu s$)
  - between CPU and GPU or
  - between multiple SMs in the GPU



PREM on GPU: Early approach – GPUguard (ETHZ)



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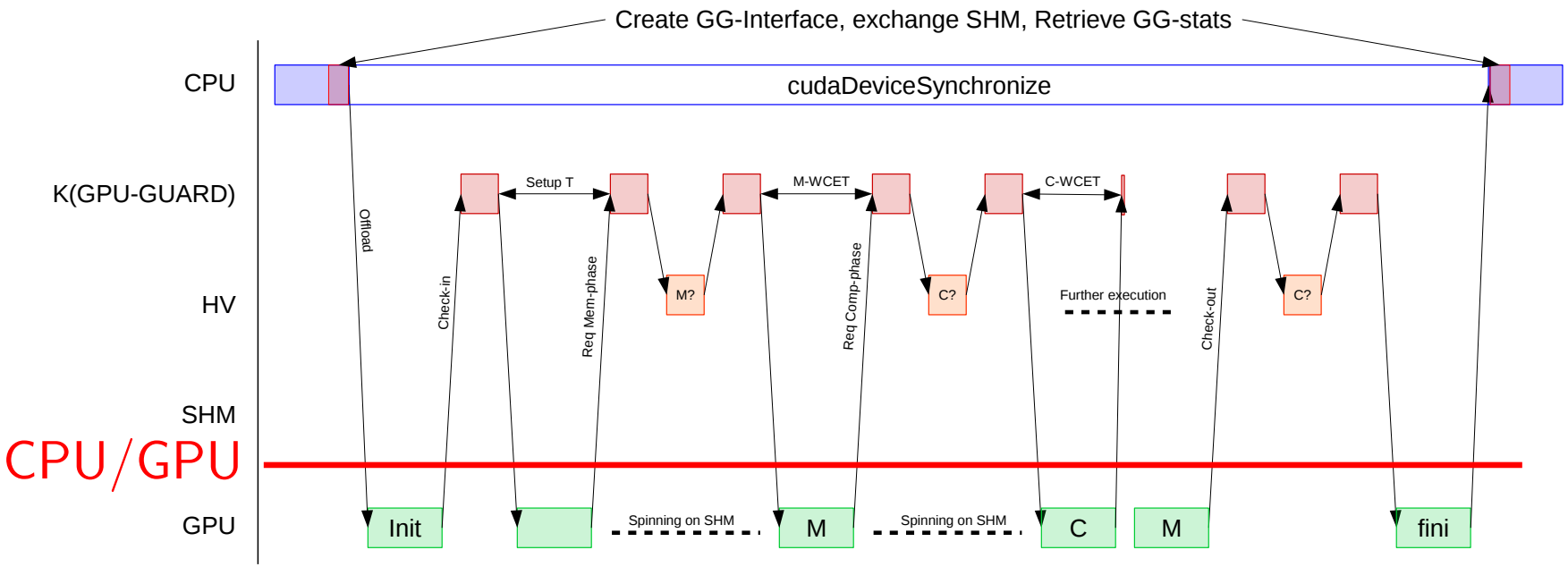

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Another approach: Time-Triggered scheduling

- GPU jobs are often offloaded in batches (e.g. one video frame)
  - the whole batch can be scheduled
  - all parameters are known at least at offload time
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  - Reduced by our approach

Outline

Overview

Interference	Approach	When
CPU-CPU	PREM and TT scheduling	past

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Experiments:

1. Synchronization overhead
2. Inter-kernel interference (2D convolution)
3. Detailed interference characterization (2D convolution)

Synchronization between GPU jobs/kernels

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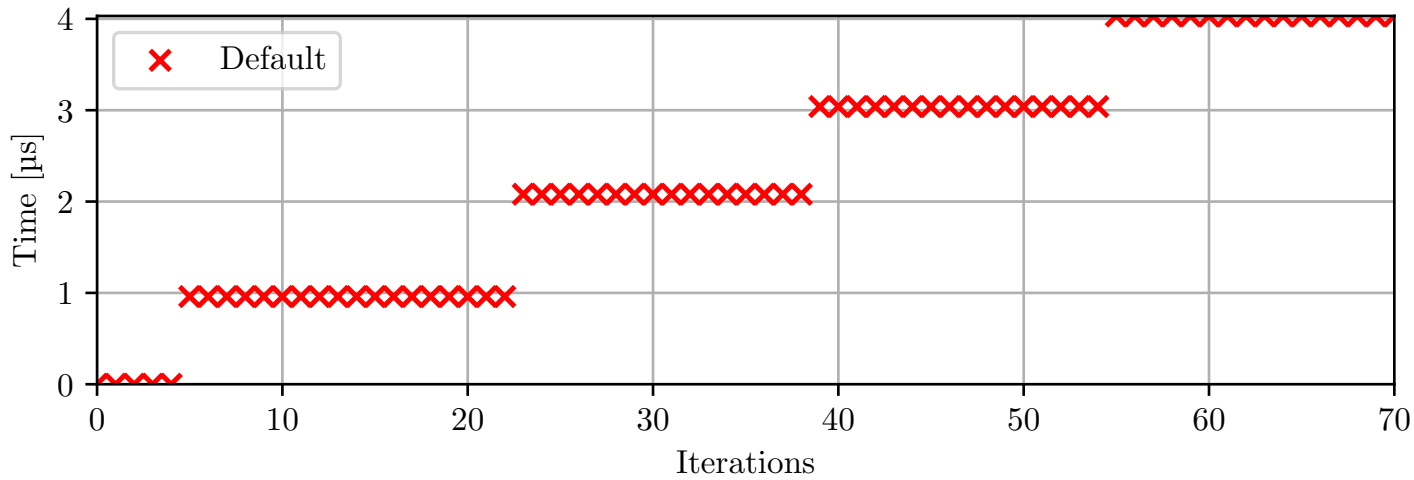

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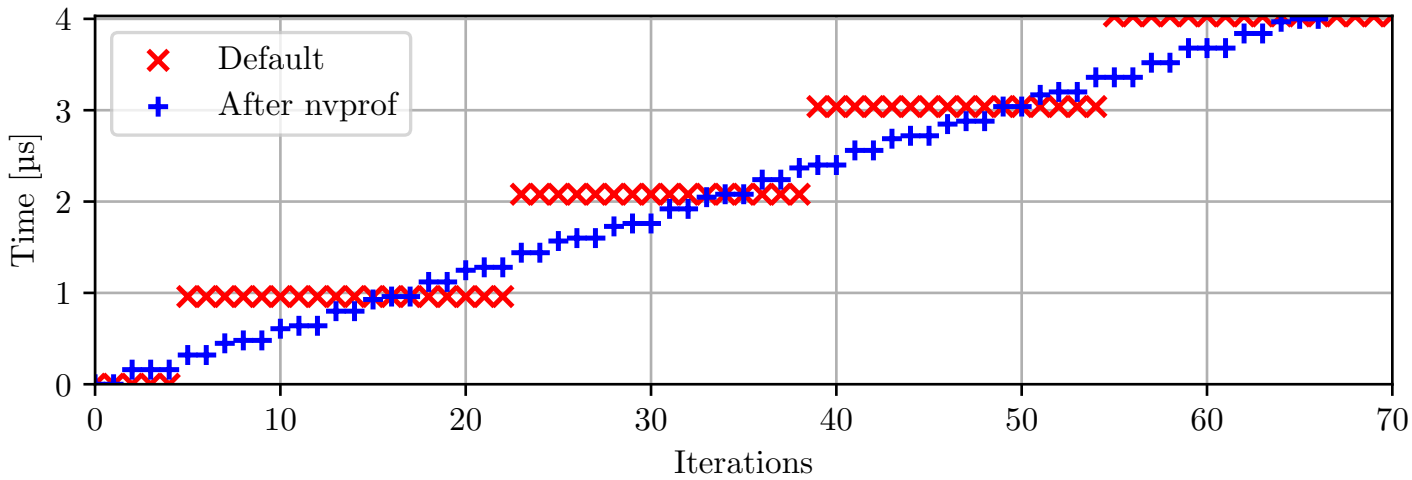
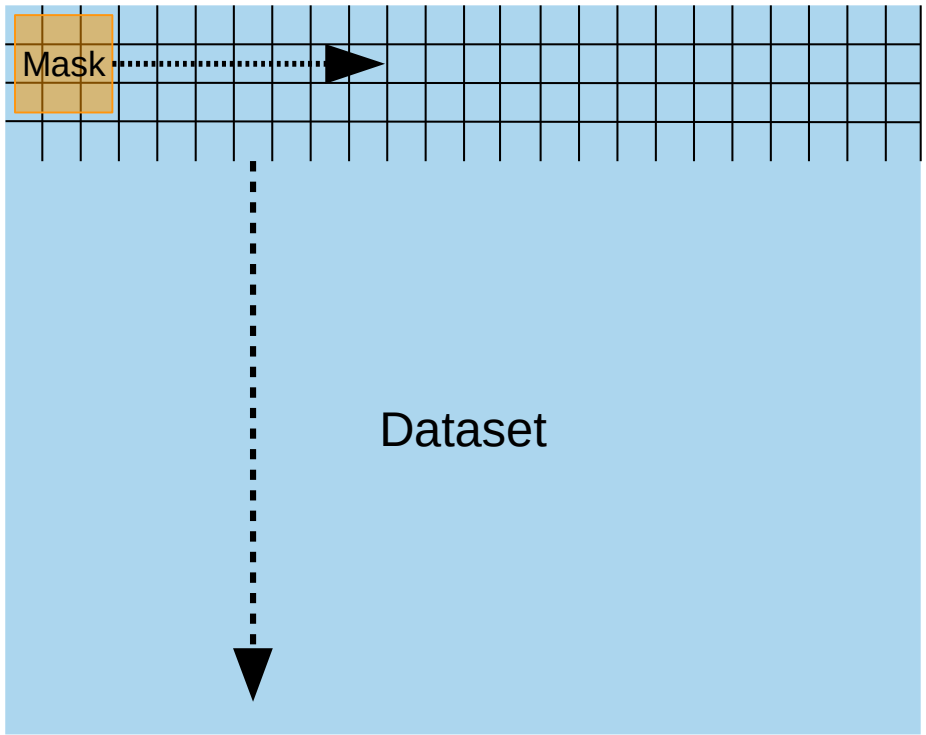


  - Default timer resolution is not sufficient: 1 µs
  - nvprof recofigures the resolution to about 160 ns

2D convolution benchmark

From Polybench-ACC benchmark suite



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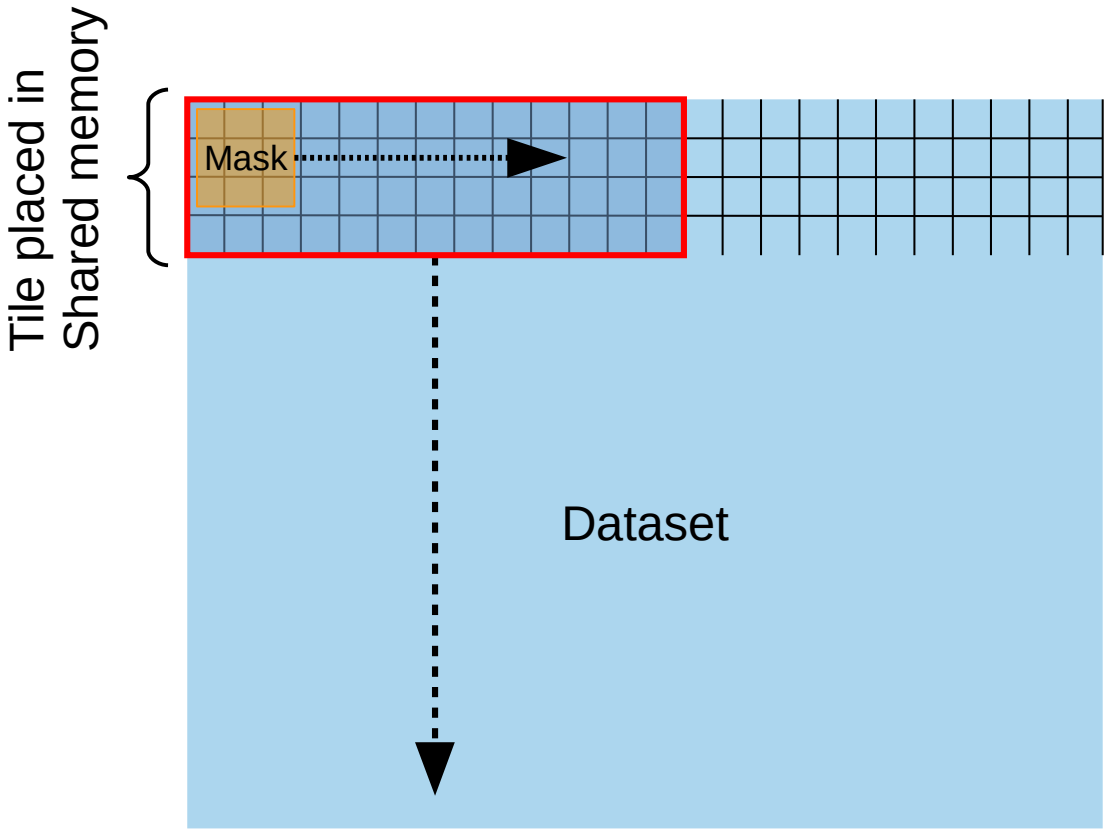

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- Tiled implementation with prefetching
  - Tile size $\Rightarrow$ 4 kernels can run simultaneously

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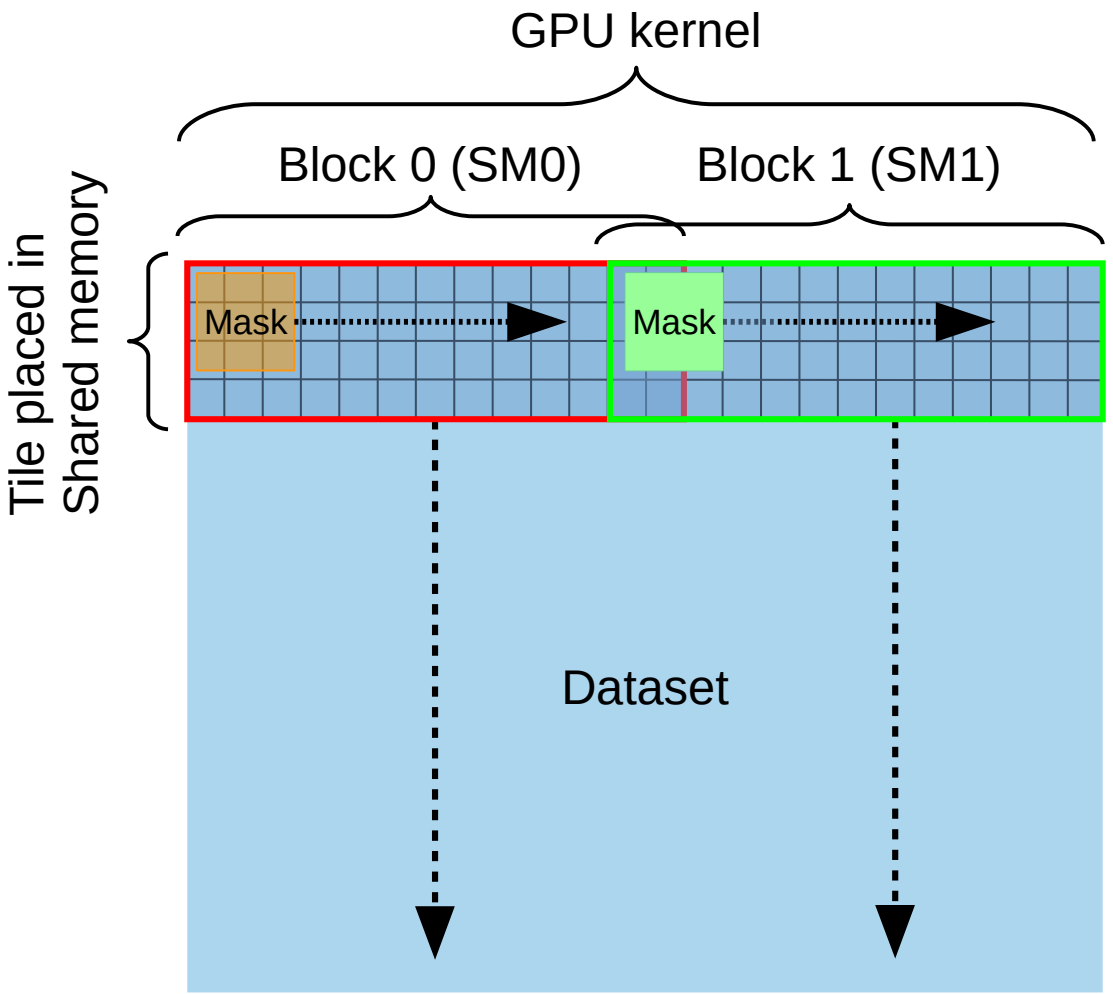

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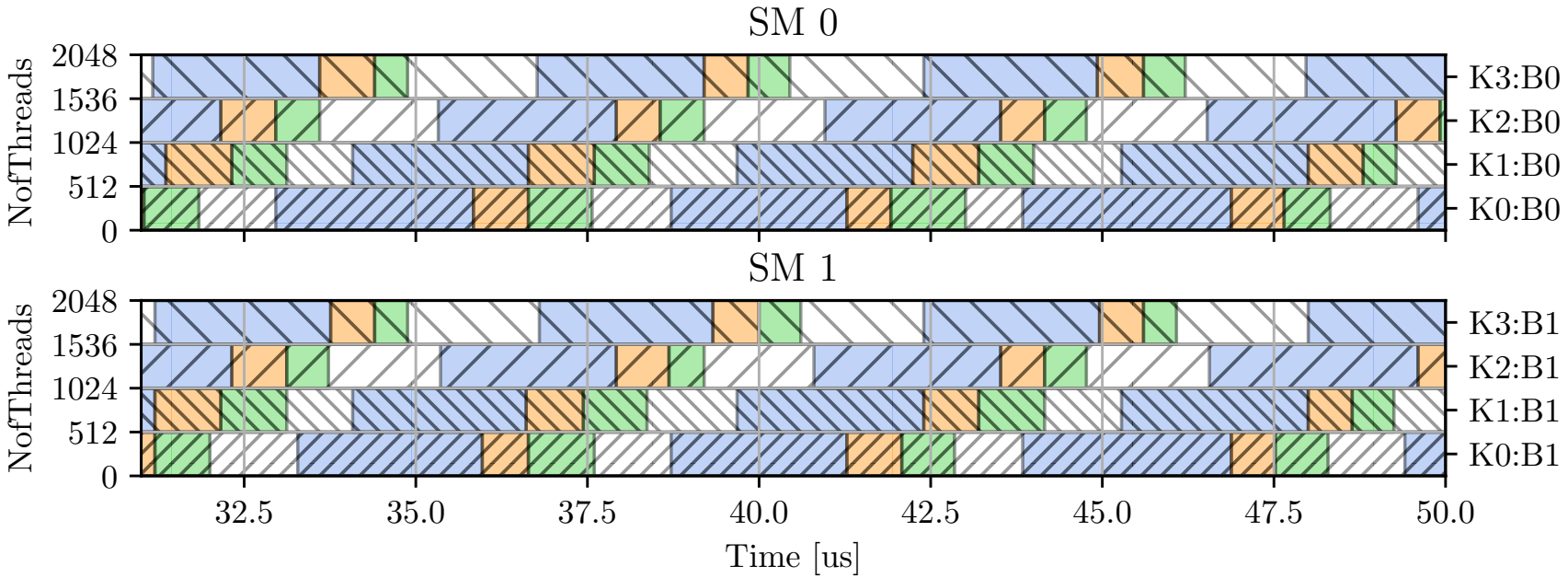
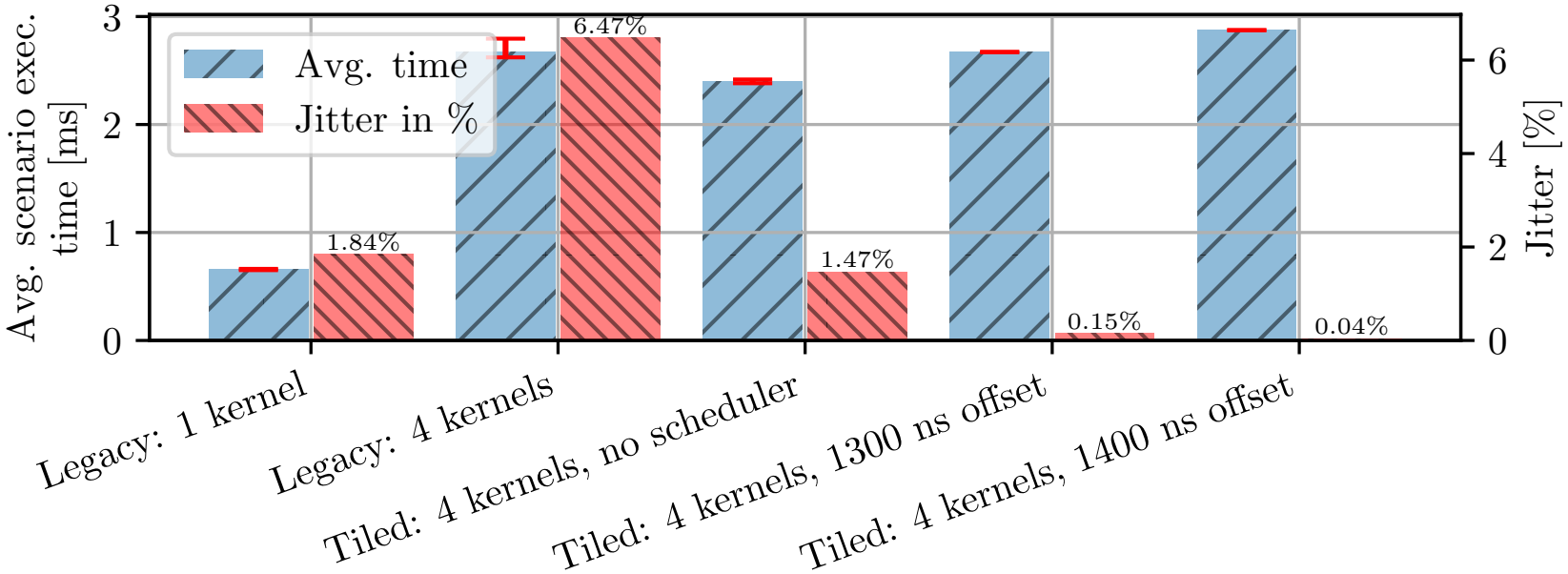
Tiled 2D convolution schedule

- 4 kernels, 2 streaming multiprocessors
- prefetch, compute, writeback phases + spinning
- different kernels started with different offsets



Results: Execution + jitter



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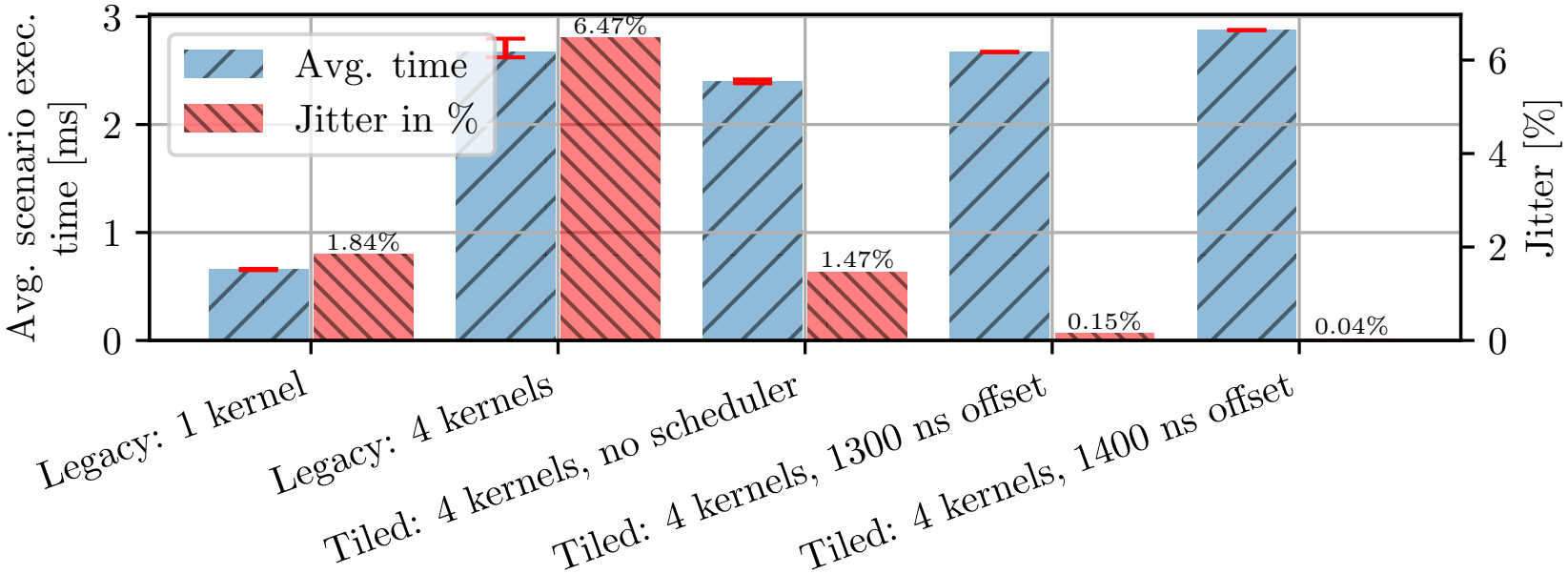
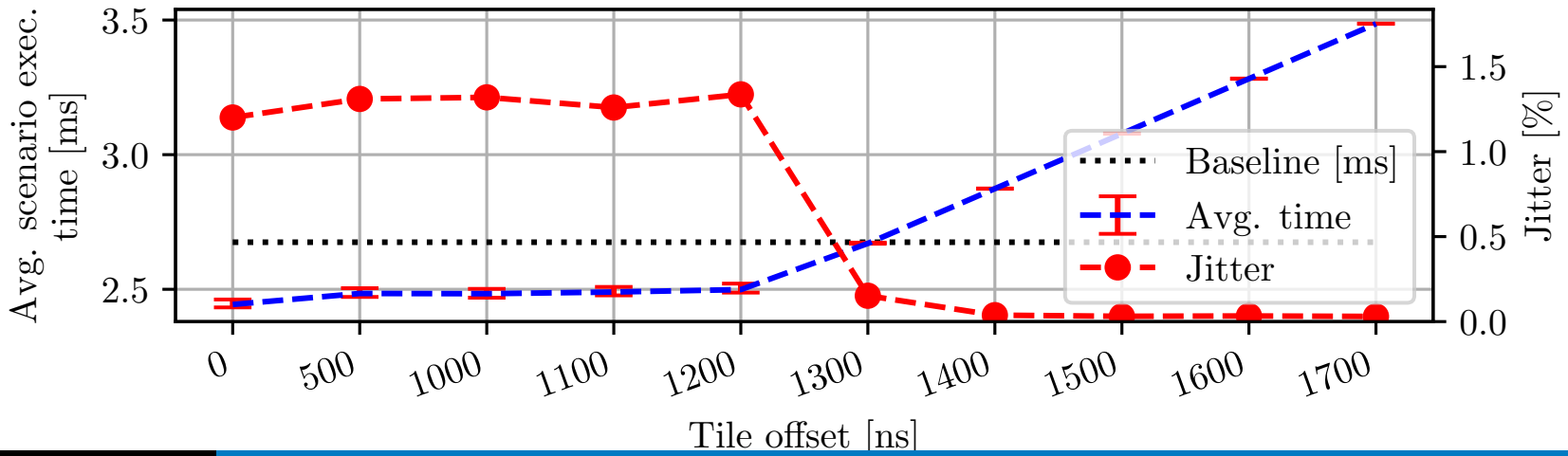
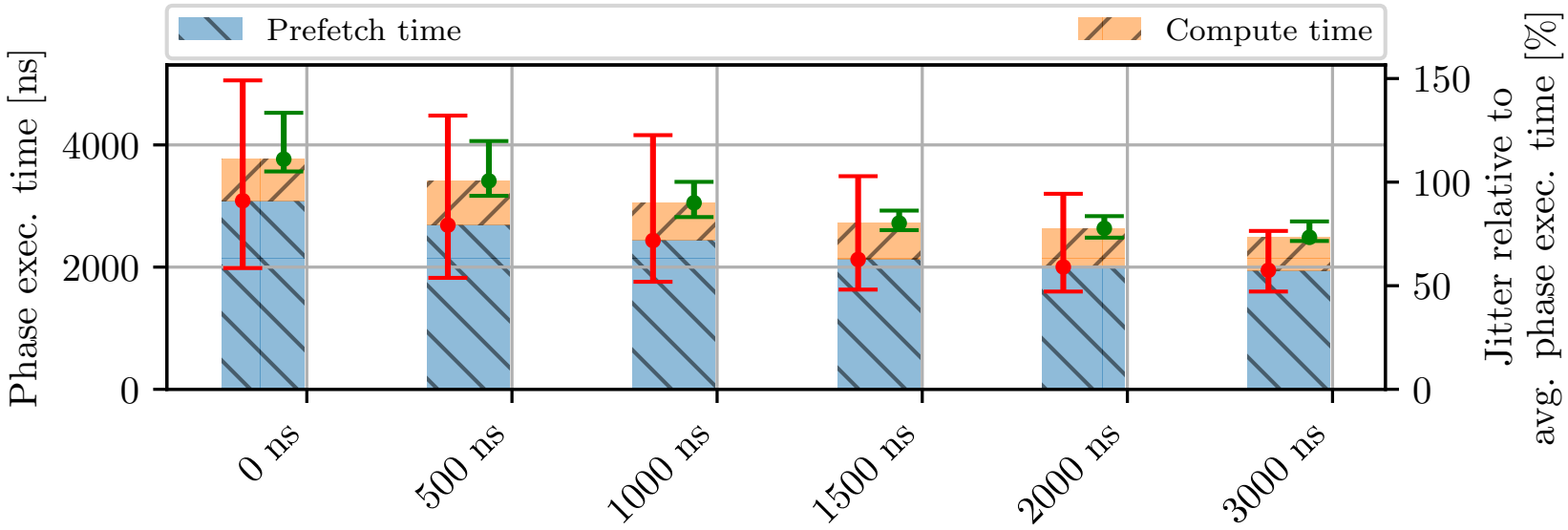




Interference between prefetch and compute phases



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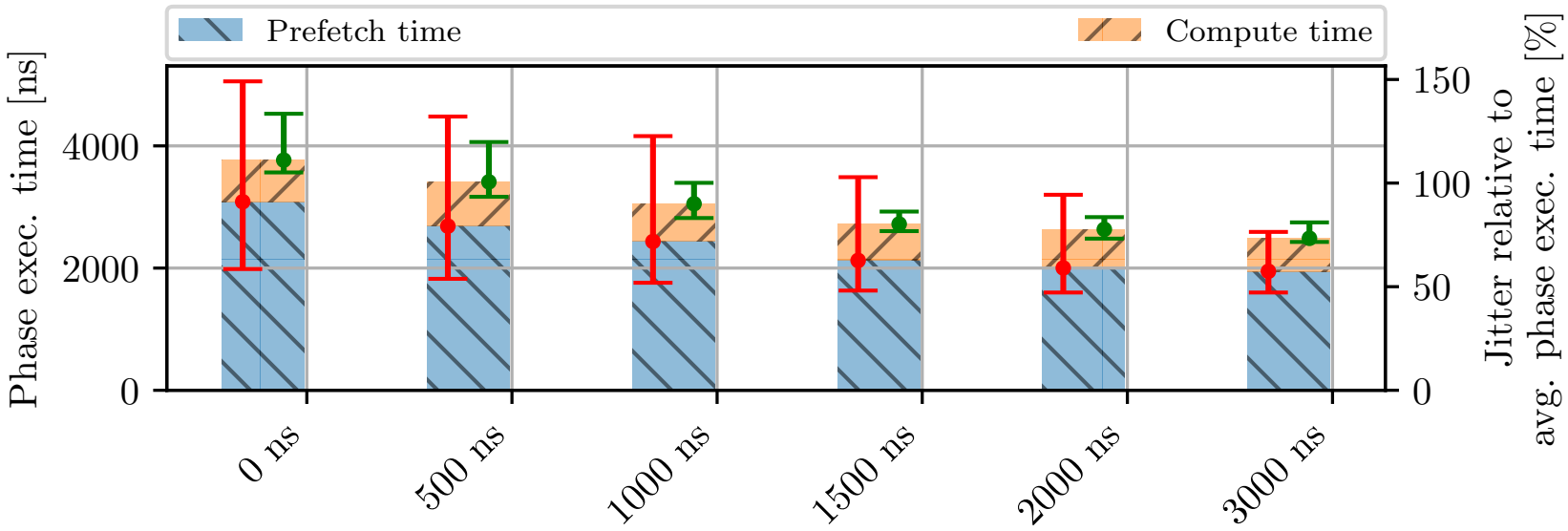

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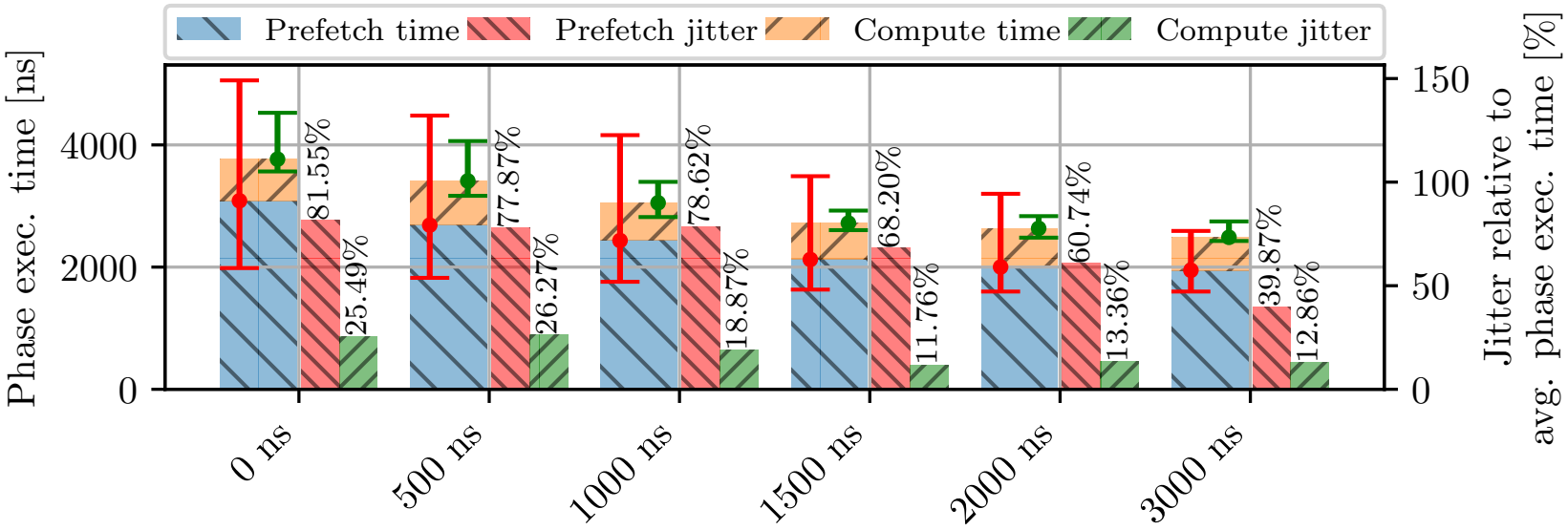

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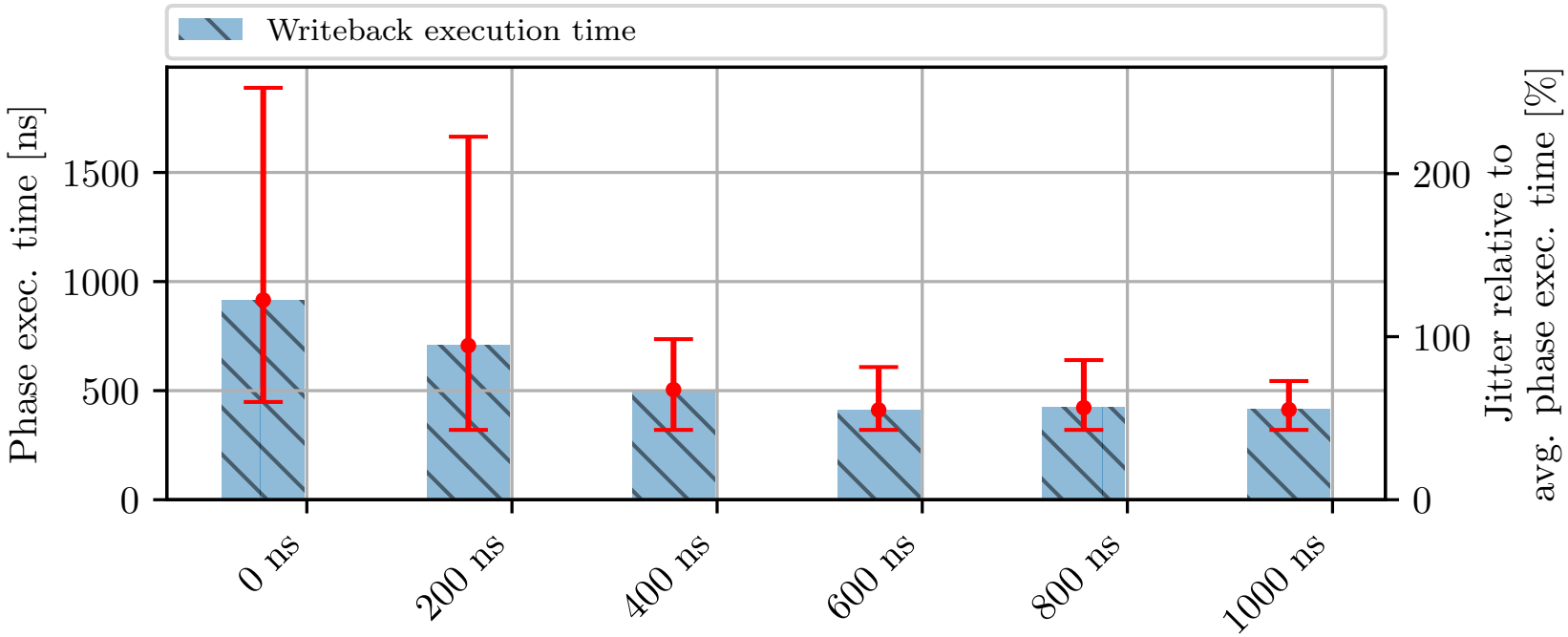

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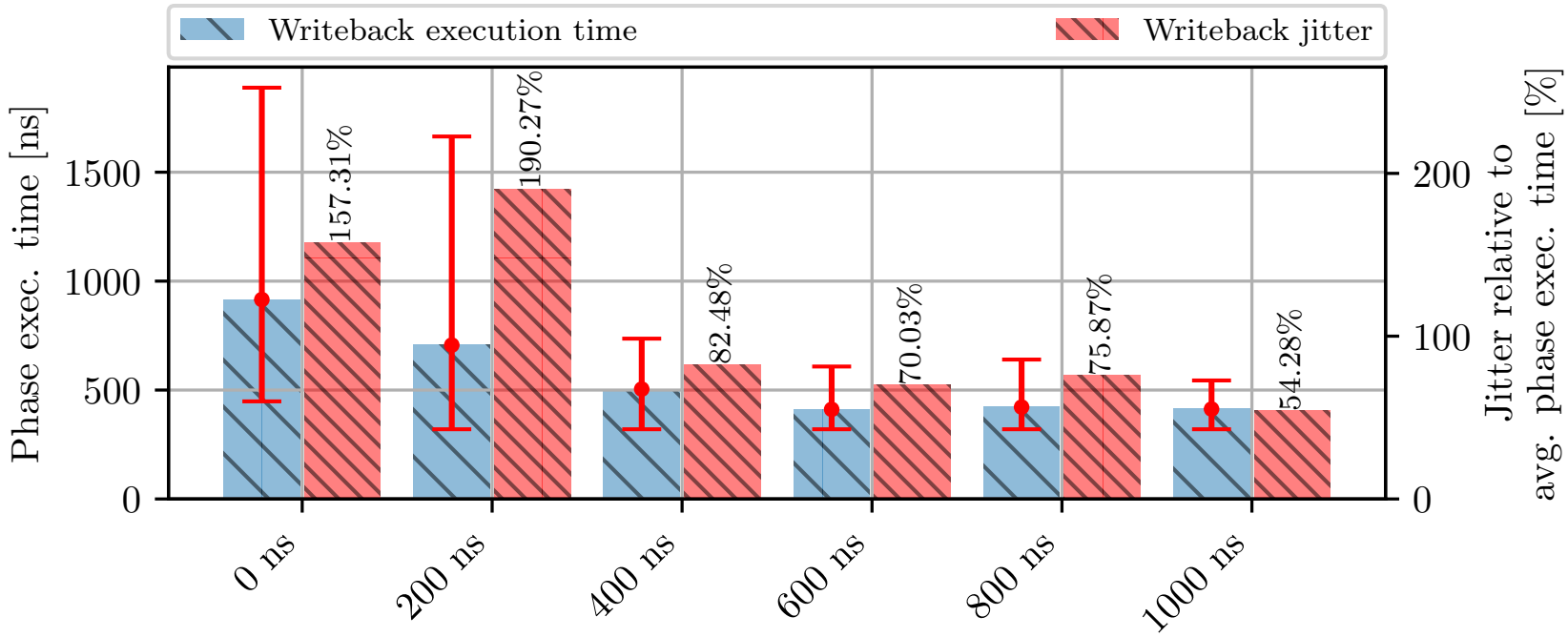

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- GPU `globaltimer` register has sufficient resolution (160 ns) after running `nvprof`
- Even very simple scheduling (adding offset) shows potential to reduce execution time jitter

Future work: Interference-aware scheduling of complex GPU workloads