Hardware-Assisted Energy Consumption Evaluation Tool for Multi-core Embedded Systems

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Outline

- Introduction
- Related Work
- REALprof: Our Proposed Solution
- Implementation and Evaluation
- Conclusions and Future Work

Introduction

- Powerful embedded systems become popular
  - multi-core
  - full-scale OS
- Energy consumption is a critical issue for embedded systems, especially for these high-end systems
- The energy consumption evaluation tools are highly demanded
  - SoC design phase
  - system integration phase
  - end product phase

Related Work

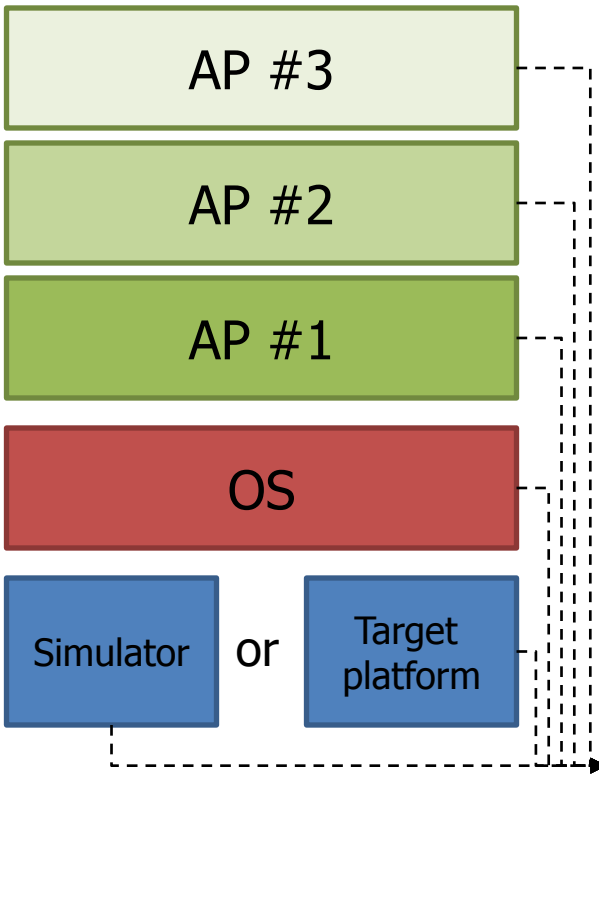
- Model-based
  - SoC design phase
  - system integration phase
  - end product phase

- Measurement-based
  - system integration phase
  - end product phase

In this paper, we consider a SoC design phase tool and a model-based approach

Model-based Approaches

3W	0.2W	0.3W	0W
5W	0.8W	1.1W	1.5W
4W	2.1W	1.3W	0.4W
2W	0.2W	0.2W	0.1W



$$E_{cpu} = E_{iexec} \times N_{iexec} + E_{dca} \times N_{dca} + P_{icpu} \times T_e$$

$$E_{sdram} = E_{dcm} \times N_{dcm} + E_{dtm} \times N_{dtm} + P_i \times T_e$$

$$P_{sp} \times T_{sp} + \beta NP_{st} \times T_{st} + \gamma NP_i \times T_i + (1-\alpha-\beta-\gamma) nP_a \times T_a$$

Model-based Approaches

- Gate-level and circuit-level simulations
  - Synopsys HSPICE and Synopsys PrimeTime
- Architecture-level simulations
  - Wattch and EMSIM

- Require considerable simulation time for evaluating complex embedded systems
  - why not utilize hardware speedup

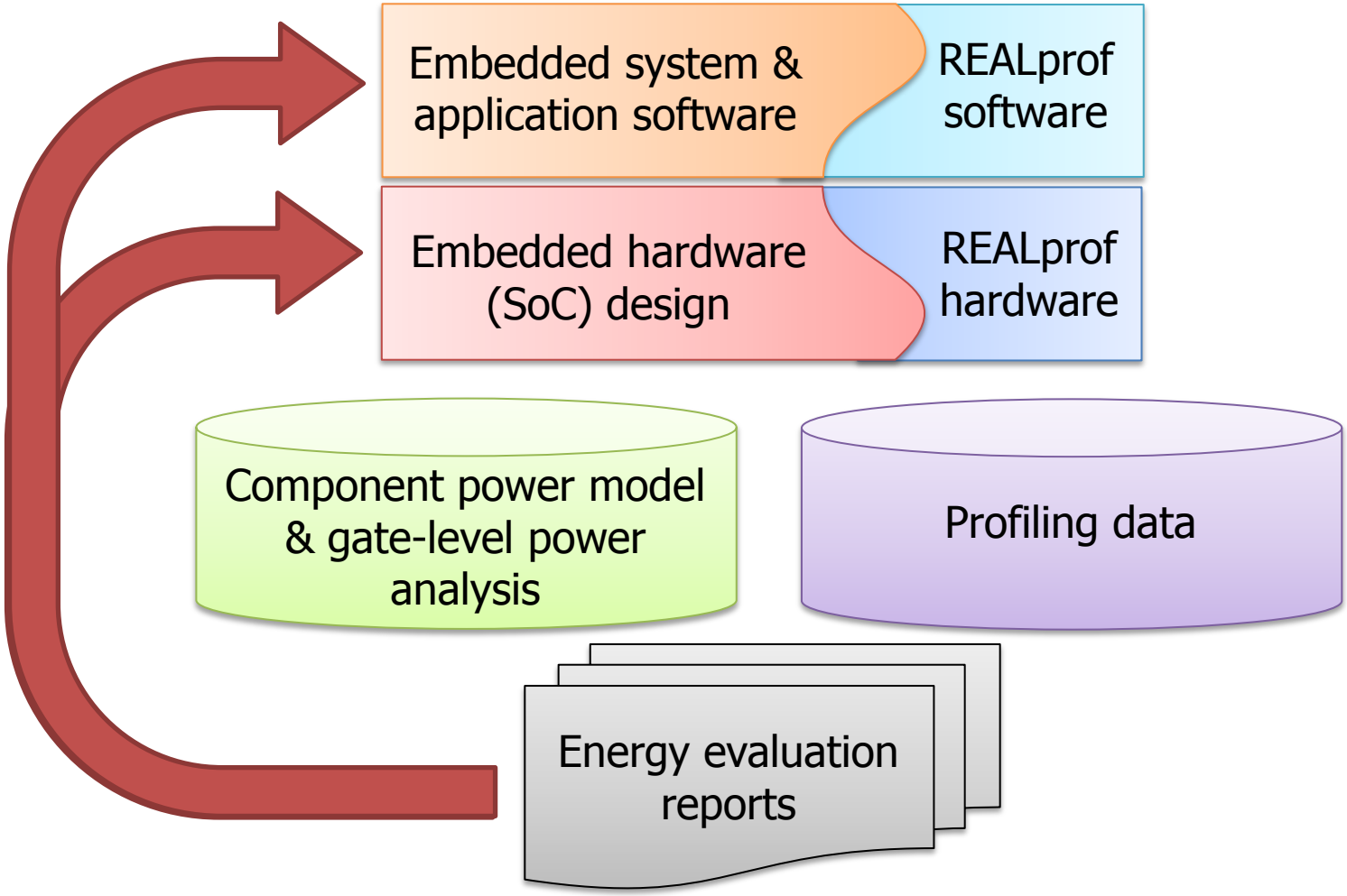
Model-based Approaches with Hardware Speedup

- Utilize hardware performance and energy counters/registers in evaluating the power consumption of the system
  - need target SoC supports
    - SoC design-in counters/registers
  - introduce considerable profiling software tool overheads

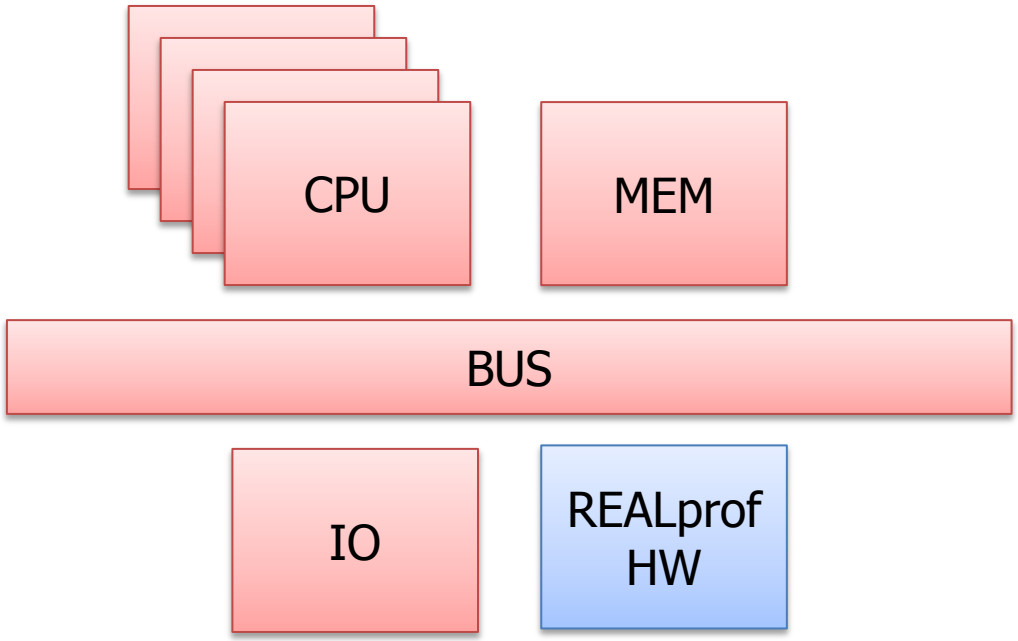
Our Solution

- Reconfigurable hardware-assisted log profiler (REALprof)
  - SoC design phase tool
  - model-based approach
  - reconfigurable profiling hardware
    - A profiling hardware module which can be easily integrated into the target design
    - static and run-time re-configurability at different profiling granularities
  - hardware logs instead of software sampling
    - Minimize the software profiling overheads

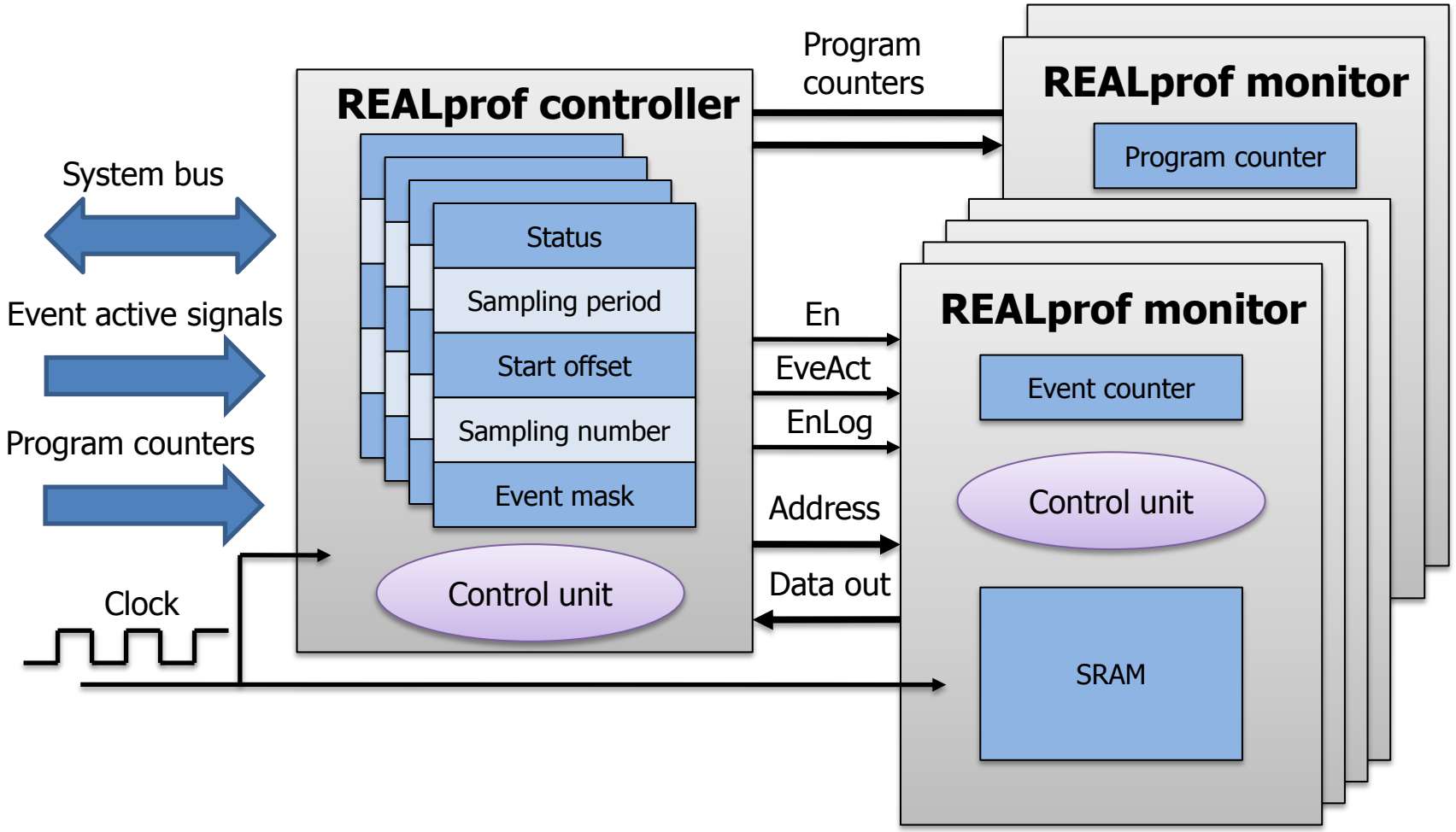
Design Flow based on REALprof



REALprof Hardware Design



REALprof Hardware Design



REALprof Software Design

- Can configure event logs/parameters at the run-time

Register	Description
Status	Control status of a REALprof monitor
Sampling Period	Sampling period of a REALprof monitor
Start Offset	Start time for profiling in number of delay cycles for a REALprof monitor
Sampling Number	Number of samples for a REALprof monitor
Event Mask	Enable/disable of a REALprof monitor

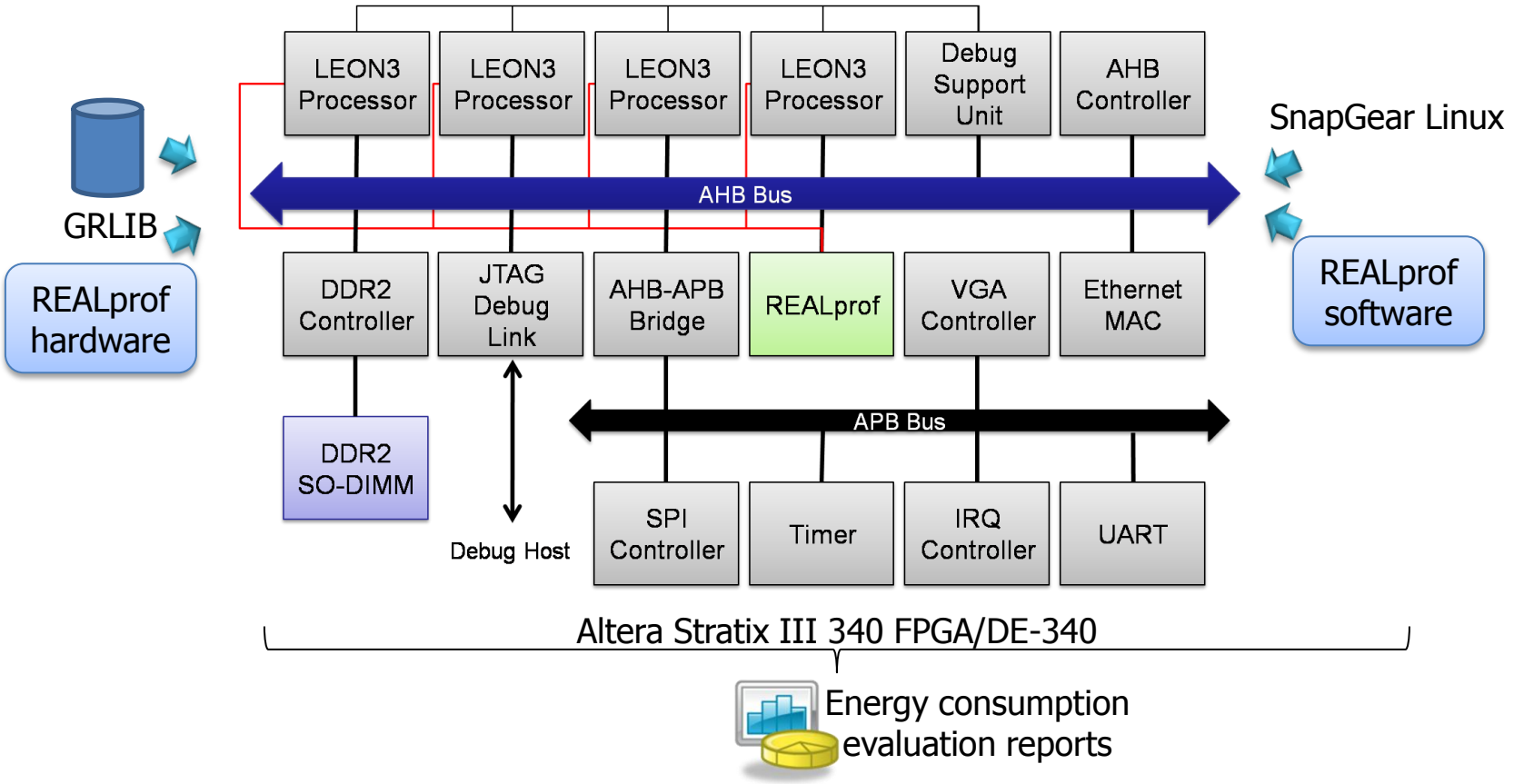
- Off-line calculation based on hardware (event) logs and power models

$$E = P_{idle} \cdot T_{total} + \sum_{i=1 \text{ to } I} E^{i}_{event} \cdot C^{i}_{event}$$

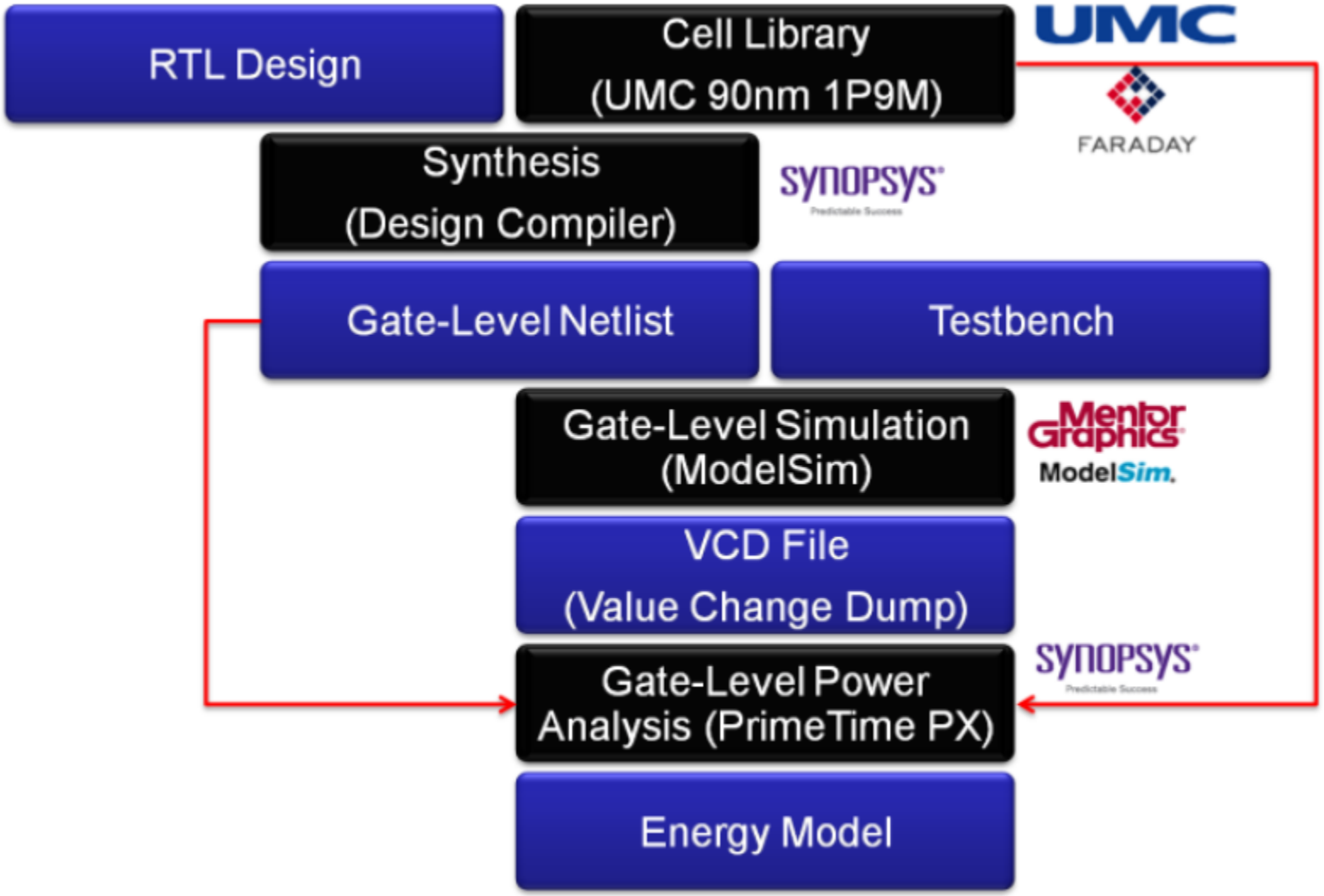
Event Logs/Parameters Examples

Component	Event	Energy/Power
Pipeline	Power down	16.1 mW
	Idle	49.2 mW
	Normal	58.2 mW
	Multiplication operation	32 pJ
	Division operation	218.75 pJ
	Instruction TLB miss	4.25 pJ
	Data TLB miss	4.25 pJ
Instruction cache	Power down	0.4084 mW
	Idle	49.1 mW
	Flush	16.403 nJ
	Hit	126.575 pJ
	Miss	123 pJ
Data cache	Idle	0.601 mW
	Flush	25.869 nJ
	Hit	314 pJ
	Miss	952.95 pJ
Register file	Idle	6.28 mW
	Single access	9.65 mW
	Double access	12.9 mW

Implementation and Evaluation



Component power model & gate-level power analysis



LEON3 Events

Component	Event	Energy/Power
Pipeline	Power down	16.1 mW
	Idle	49.2 mW
	Normal	58.2 mW
	Multiplication operation	32 pJ
	Division operation	218.75 pJ
	Instruction TLB miss	4.25 pJ
	Data TLB miss	4.25 pJ
Instruction cache	Power down	0.4084 mW
	Idle	49.1 mW
	Flush	16.403 nJ
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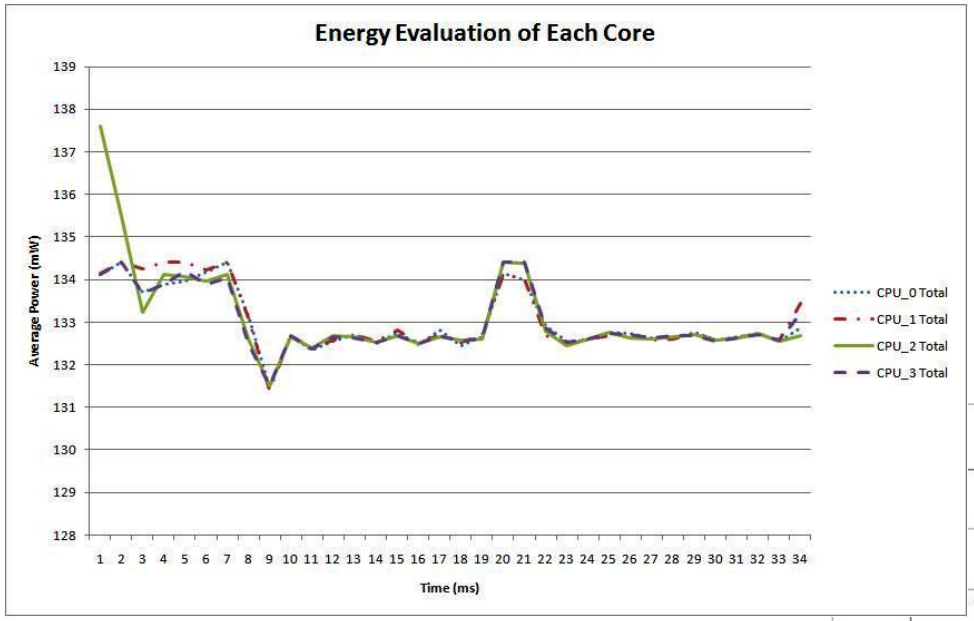
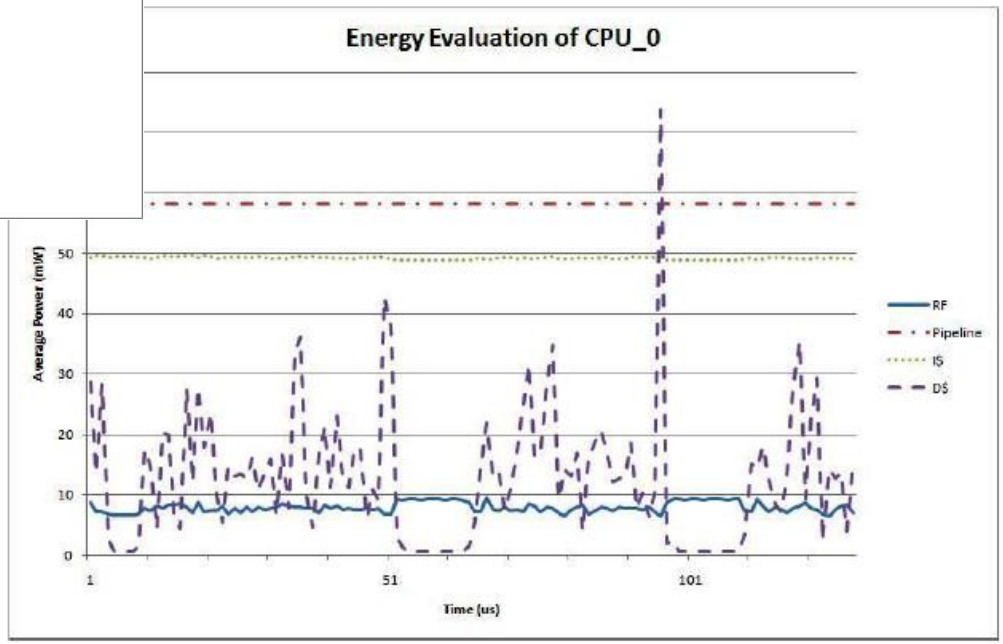
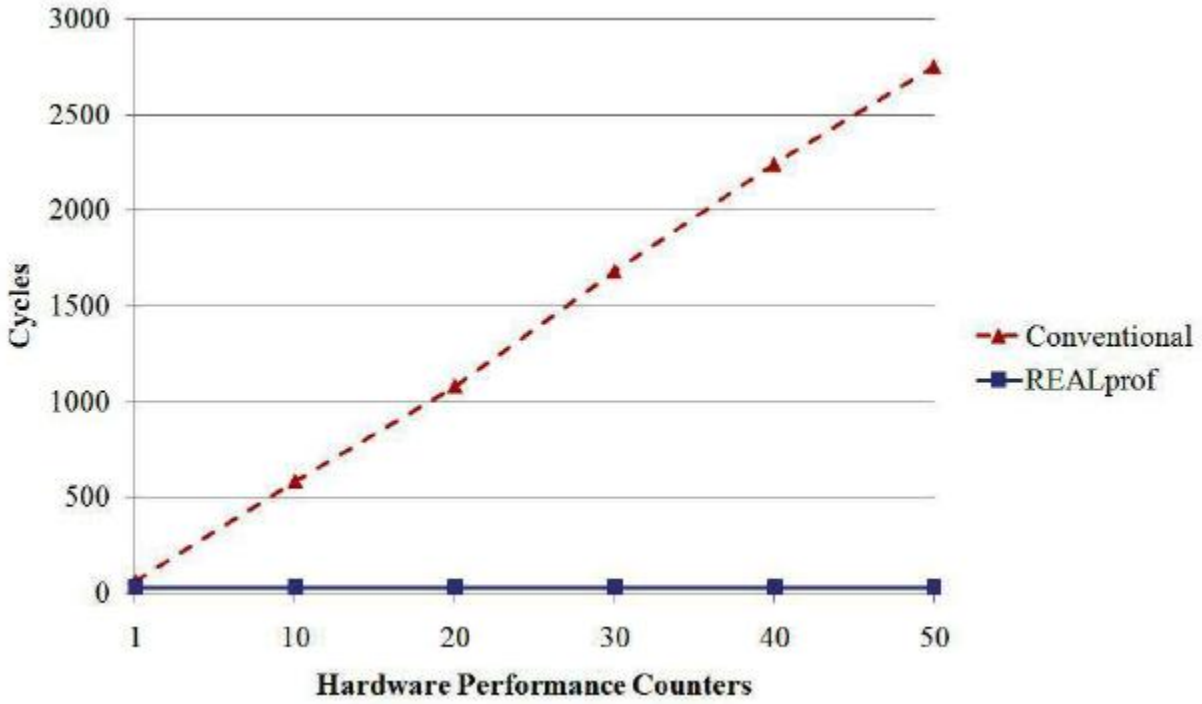
Detailed Power Consumption Evaluation



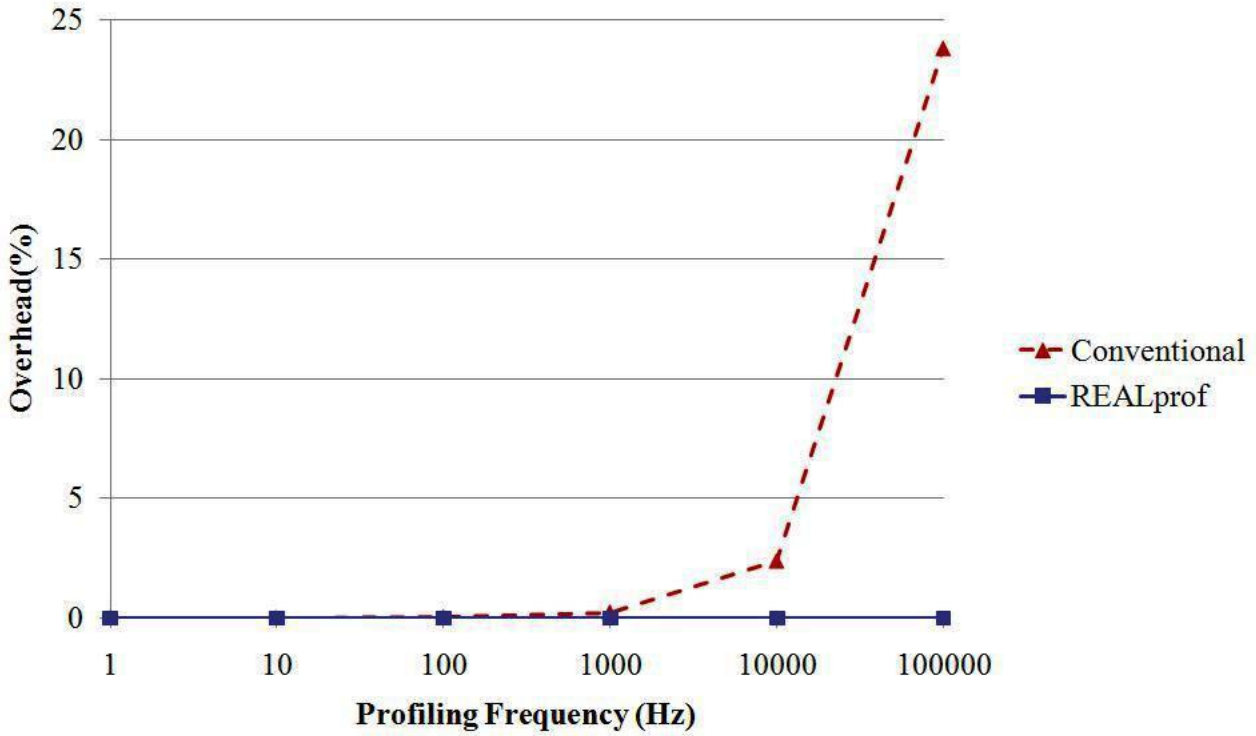


Profiling Overheads

- Overhead comparison between architecture-level simulations and REALprof



Profiling Overheads



Comparisons

	REALprof	Profiling based on hardware counters [12]	Architecture-level simulation [9]	Circuit-level simulation [6][7]
Method	Hardware emulation	directly execute	Software simulation	Software simulation
Speed	~ 100 MHz	real speed	KIPS ~ MIPS	extremely slow
Flexibility of profiling	Y	N	Y	Y
Profiling overhead	Negligible (less than 30 cycles)	Software profiling overhead	N/A	N/A
Profiling granularity	~30 cycles	~ millisecond	~microsecond	cycle
Profiling hardware resource	Hardware counters + RAM	Hardware counters	N	N
Program behavior while profiling	Remain unchanged	influenced	Remain unchanged	Remain unchanged
Operating system	Y	Y	usually N	N

StratixIII 340 FPGA Resource Usage

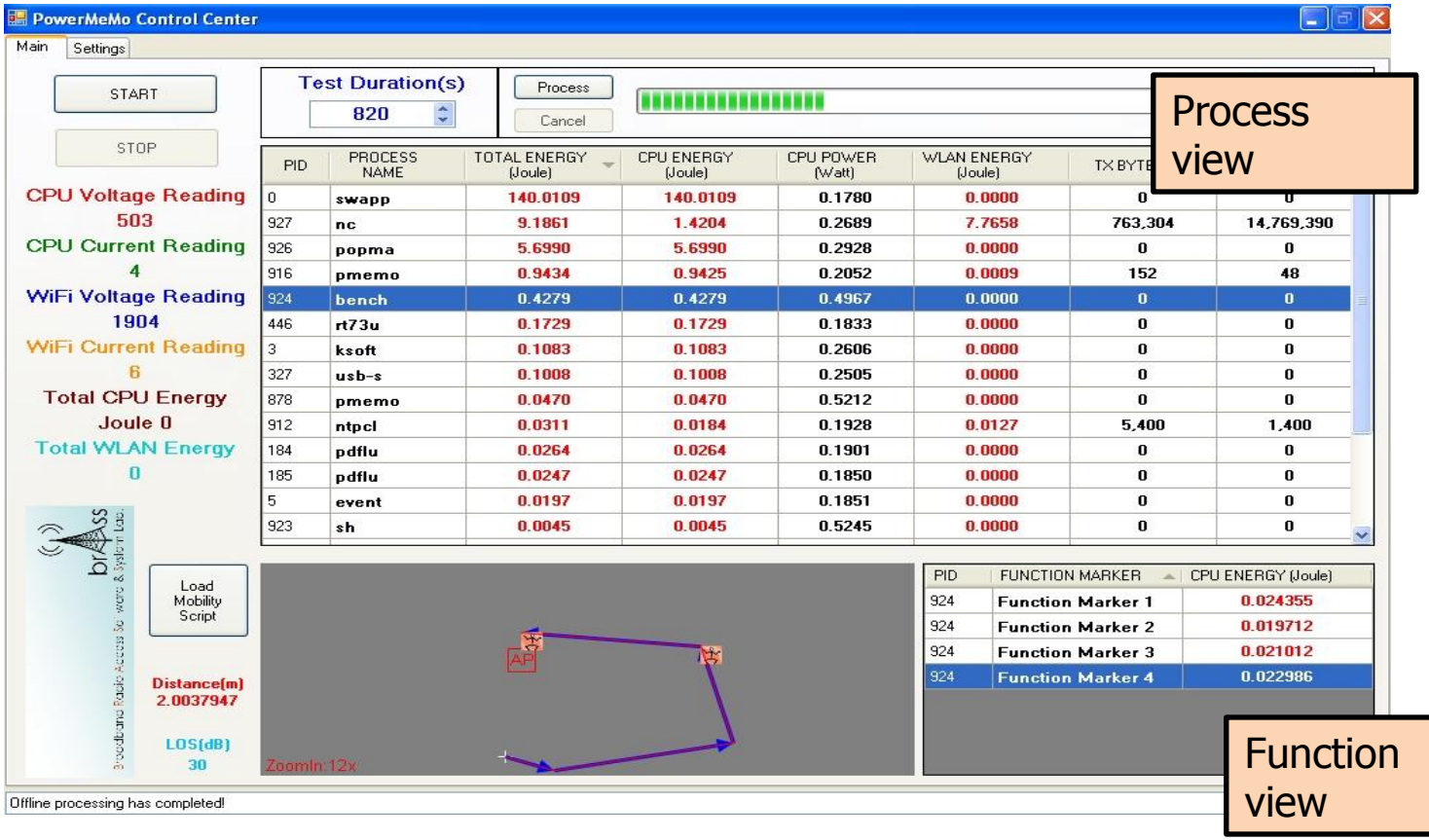
	Combinational ALUTs	Logic registers	DSP block	Block memory bit	Number of components
LEON3 processor	12581	8451	4	343936	4
DDR2 controller	781	601	0	4096	1
peripherals	2600	1269	0	16384	N/A
REALprof	4826 (2%)	2091 (1%)	0 (0%)	557056 (4%)	1 controller 68 monitors
Total	58531 (22%)	37765 (14%)	16 (3%)	1953280 (12%)	

Conclusions and Future Work

- We proposed REALprof
  - SoC design phase tool/model-based approach/reconfigurable profiling hardware/hardware logs
- We implemented REALprof on LEON3 multi-core and Linux
- Less than 1% overhead while offering microsecond-level profiling granularity

Conclusions and Future Work

- Move from EXCEL report to GUI interface



PID	PROCESS NAME	TOTAL ENERGY (Joule)	CPU ENERGY (Joule)	CPU POWER (Watt)	WLAN ENERGY (Joule)	TX BYTE	
0	swapp	140.0109	140.0109	0.1780	0.0000	0	0
927	nc	9.1861	1.4204	0.2689	7.7658	763,304	14,769,390
926	popma	5.6990	5.6990	0.2928	0.0000	0	0
916	pmemo	0.9434	0.9425	0.2052	0.0009	152	48
924	bench	0.4279	0.4279	0.4967	0.0000	0	0
446	rt73u	0.1729	0.1729	0.1833	0.0000	0	0
3	ksoft	0.1083	0.1083	0.2606	0.0000	0	0
327	usb-s	0.1008	0.1008	0.2505	0.0000	0	0
878	pmemo	0.0470	0.0470	0.5212	0.0000	0	0
912	ntpcl	0.0311	0.0184	0.1928	0.0127	5,400	1,400
184	pdflu	0.0264	0.0264	0.1901	0.0000	0	0
185	pdflu	0.0247	0.0247	0.1850	0.0000	0	0
5	event	0.0197	0.0197	0.1851	0.0000	0	0
923	sh	0.0045	0.0045	0.5245	0.0000	0	0

PID	FUNCTION MARKER	CPU ENERGY (Joule)
924	Function Marker 1	0.024355
924	Function Marker 2	0.019712
924	Function Marker 3	0.021012
924	Function Marker 4	0.022986

Thanks for your attention