
Modeling Real-Time Networks with MAST2

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Modeling Real-Time Networks with MAST2



1. Introduction

2. Overview of the MAST2 model

3. Networks

4. Network switches and routers

5. Modelling AFDX networks

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1. Introduction

MAST (Modeling and Analysis Suite for Real-Time Applications)

- **defines a model to describe the timing behavior of real-time systems**
- **model is analyzable via schedulability analysis techniques**
- **sensitivity analysis**
- **assignment of scheduling parameters**
- **support for different scheduling policies**

The MAST model is very similar to the model defined in MARTE:

- **the standardized UML profile for real-time embedded systems**

Some of the new elements being defined in MAST2 are network switches and routers

- IEEE 802.1p switches with prioritized traffic
- The Avionics Full-Duplex Switched Ethernet (AFDX) defines a hard real-time network based on switched ethernet

Communications network defined in the ARINC-644, Part 7 standard

- based on the use of point to point full duplex ethernet links
- and special purpose switches

The routing of messages is preconfigured

- there is no delay in the discovery of routing addresses

Two redundant hardware communication channels

The switches can filter erroneous traffic

The switches have two FIFO queues at each output port

- high and low priority traffic

Virtual Links

Traffic regulation at the sending end via *Virtual Links*

- communication objects with a dedicated maximum bandwidth

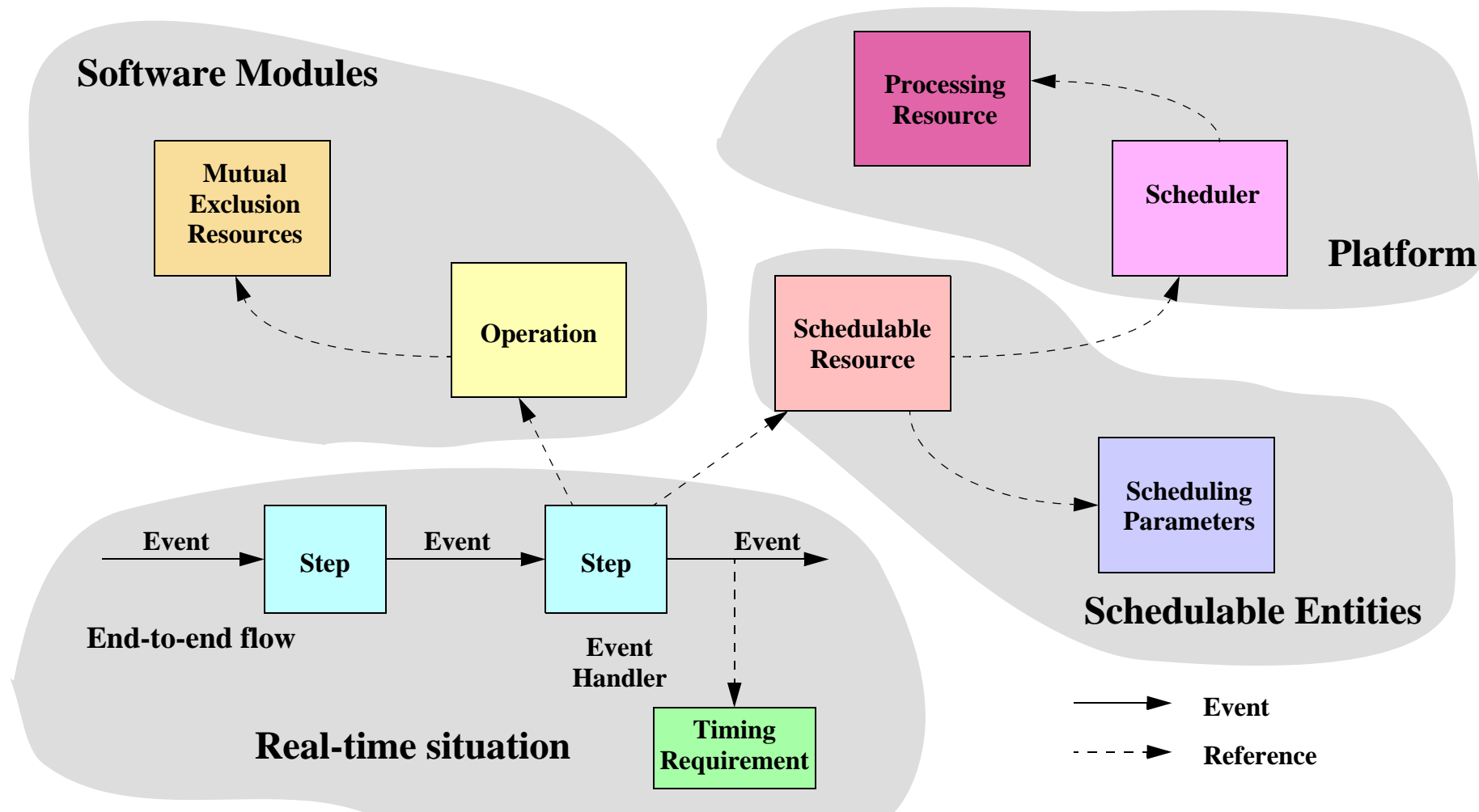
Each virtual link (VL) has two parameters

- ***Lmax***: the largest Ethernet frame in bytes
- ***BAG***: the Bandwidth Allocation Gap (*BAG*)
 - a power of the value 2 in the range [1,128] ms
 - the *BAG* is the minimum interval between Ethernet frames transmitted on the VL

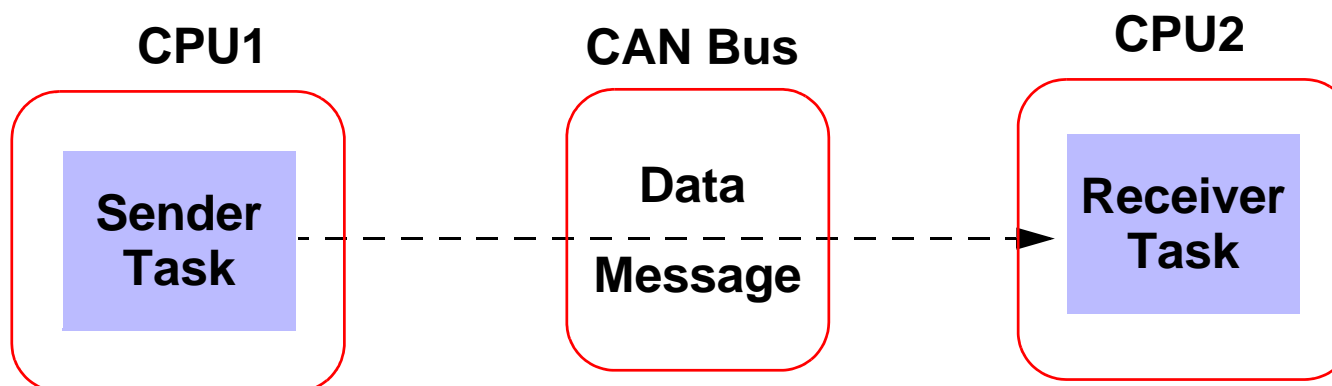
Each virtual link has a FIFO queue for all the fragmented packets to be transmitted through it

The priority is configured on a VL basis

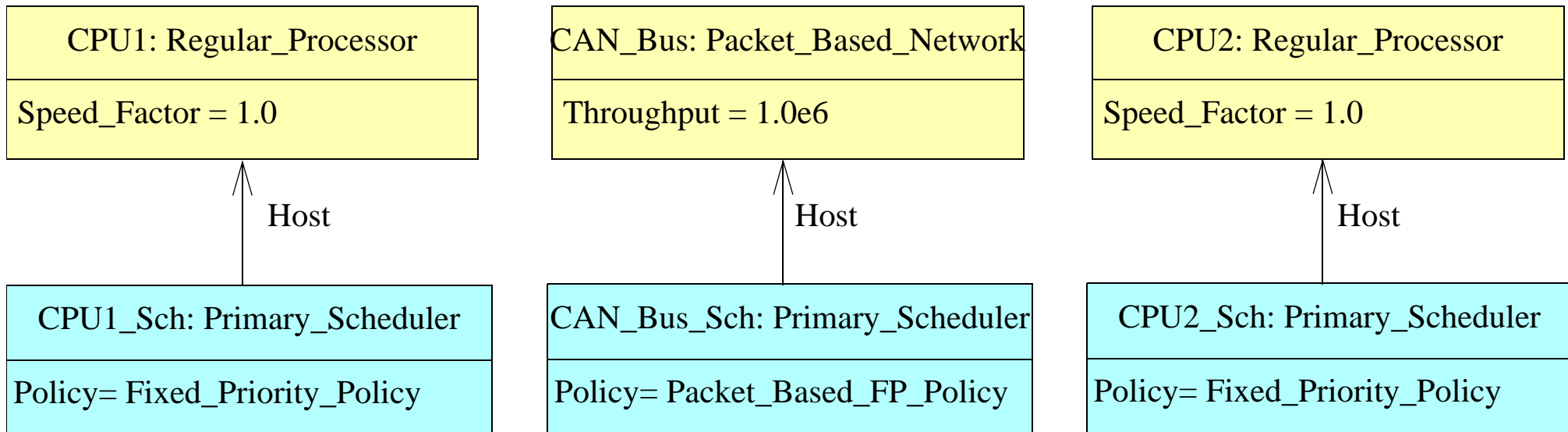
2. Overview of the MAST2 model



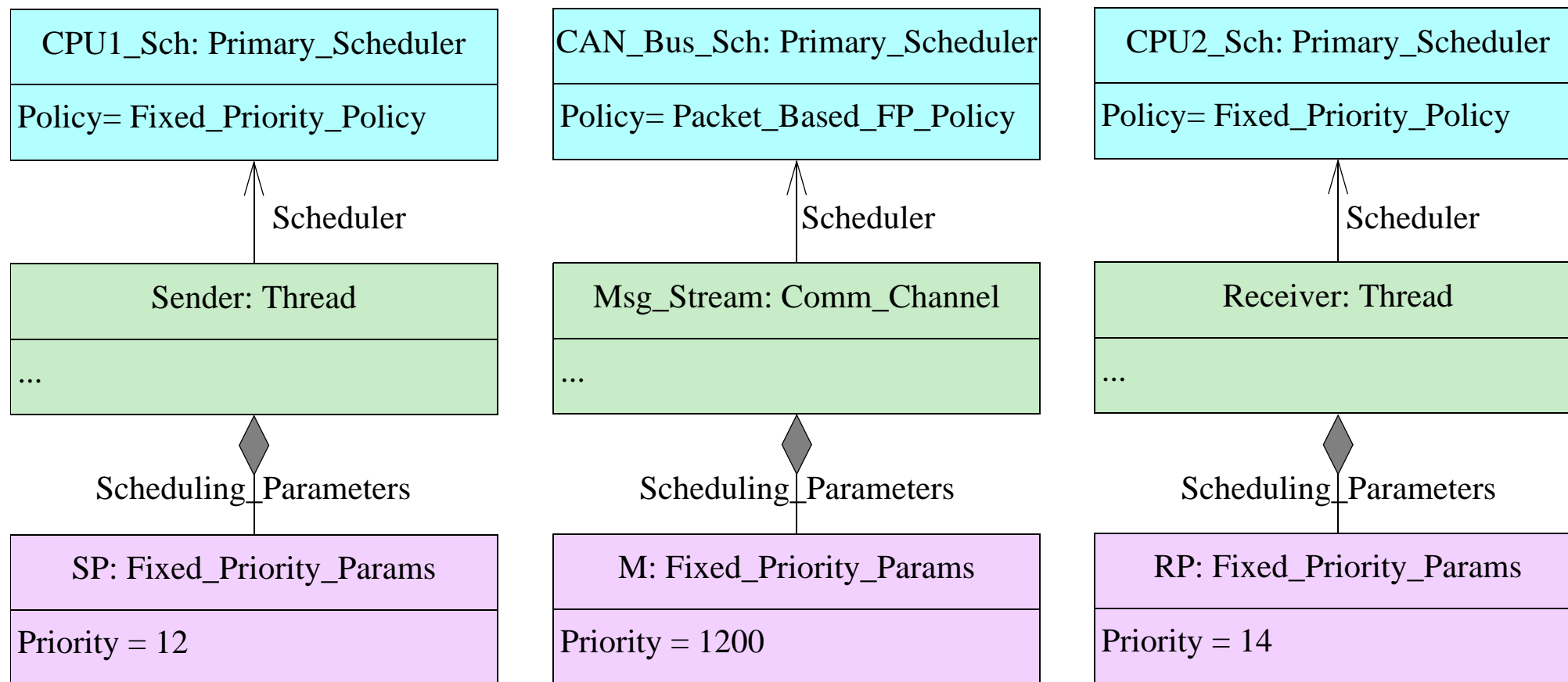
A simple distributed example



Platform View



Concurrent architecture view



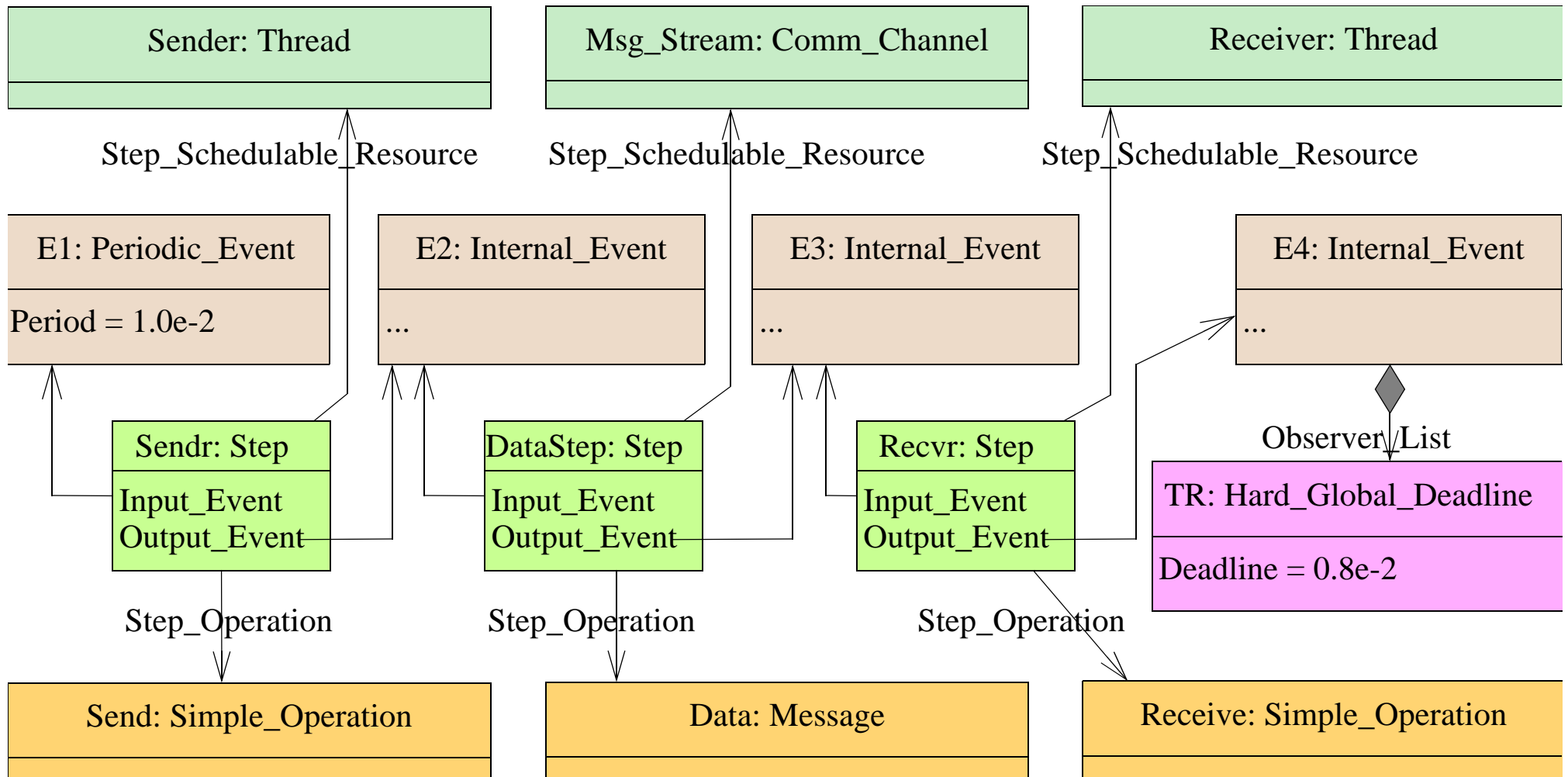
Operations view

Send: Simple_Operation
WCET = 1.23e-3

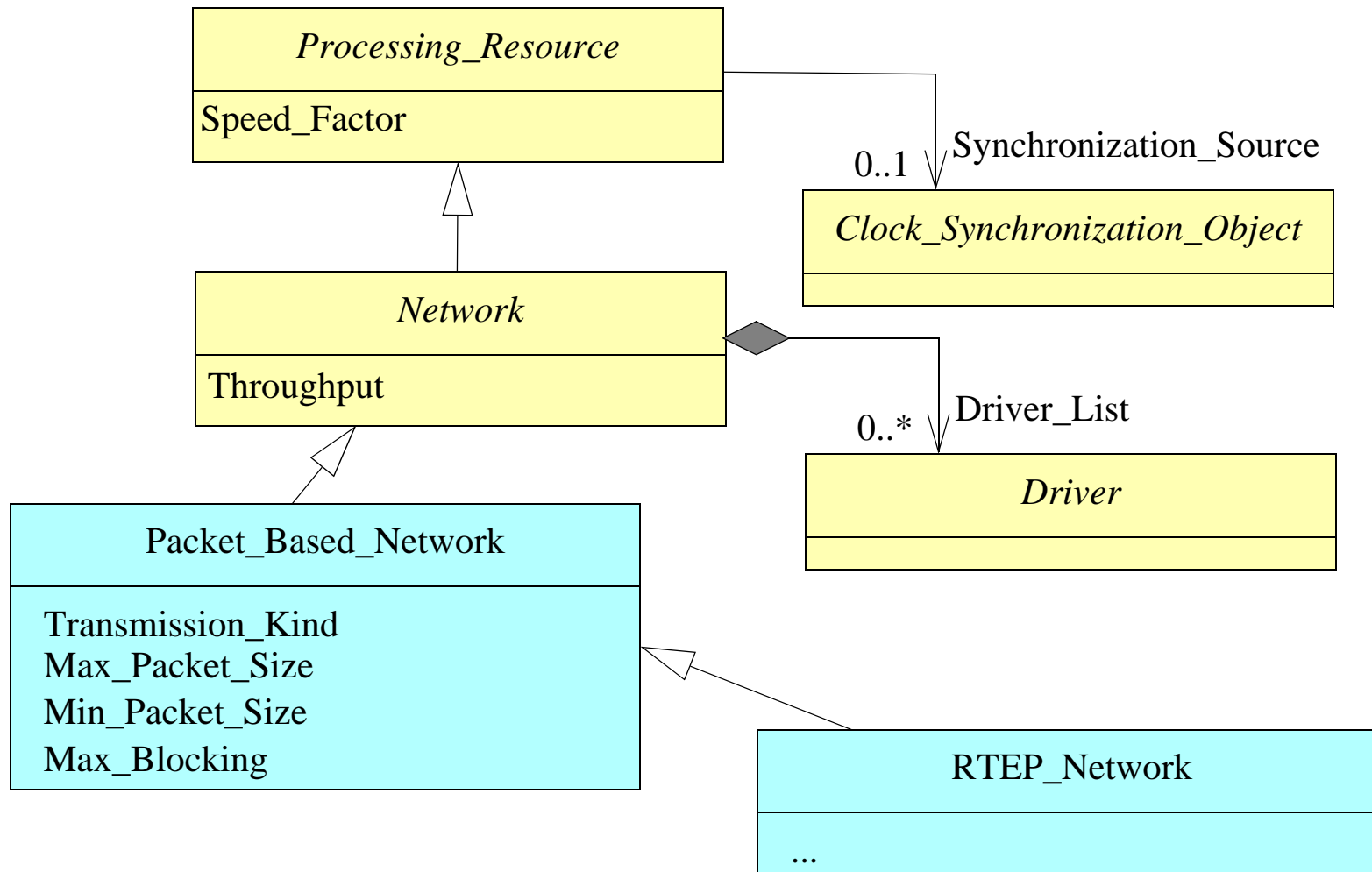
Data: Message
Max_Message_Size = 1600

Receive: Simple_Operation
WCET = 1.23e-3

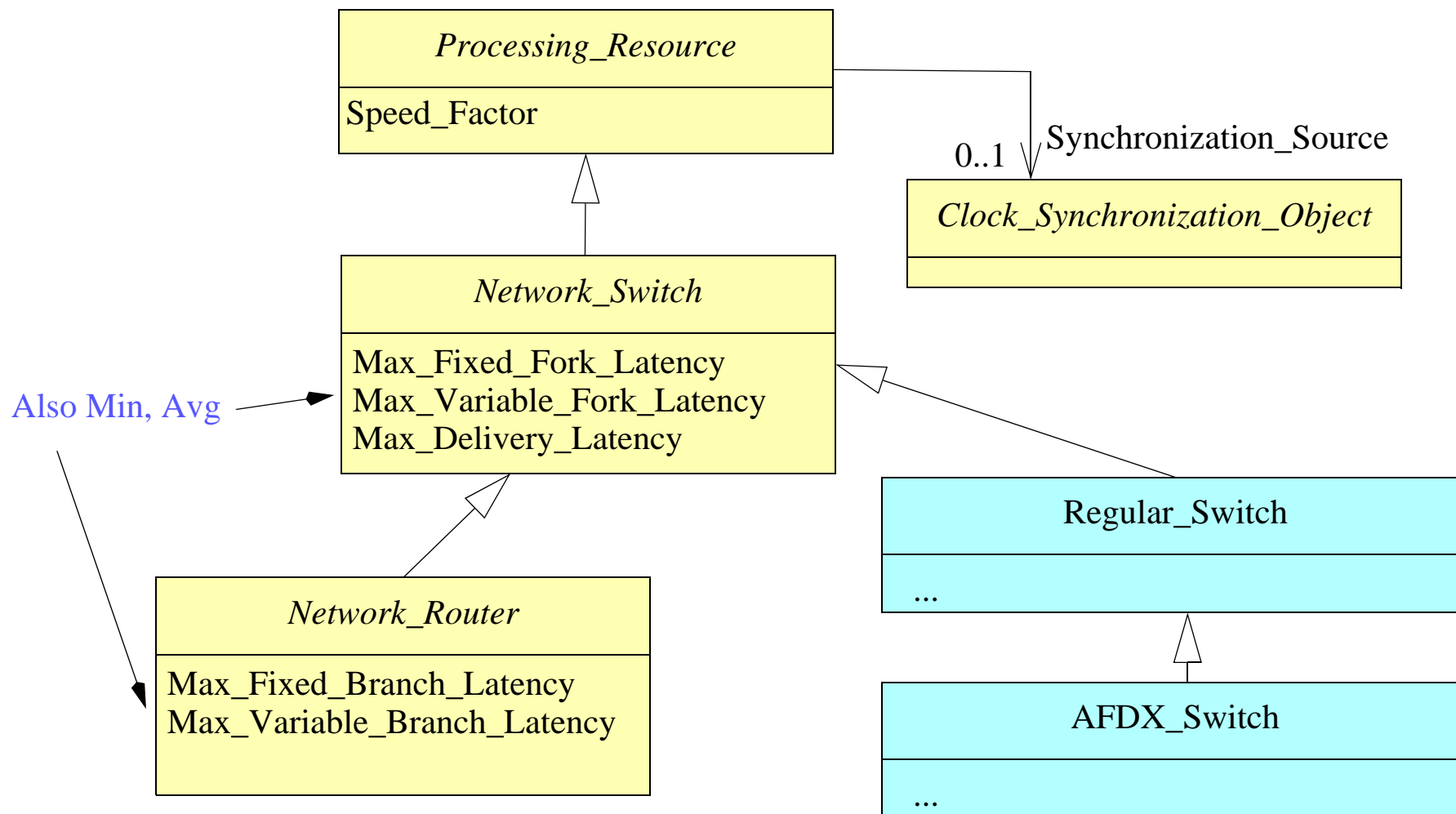
Real-Time Situation view



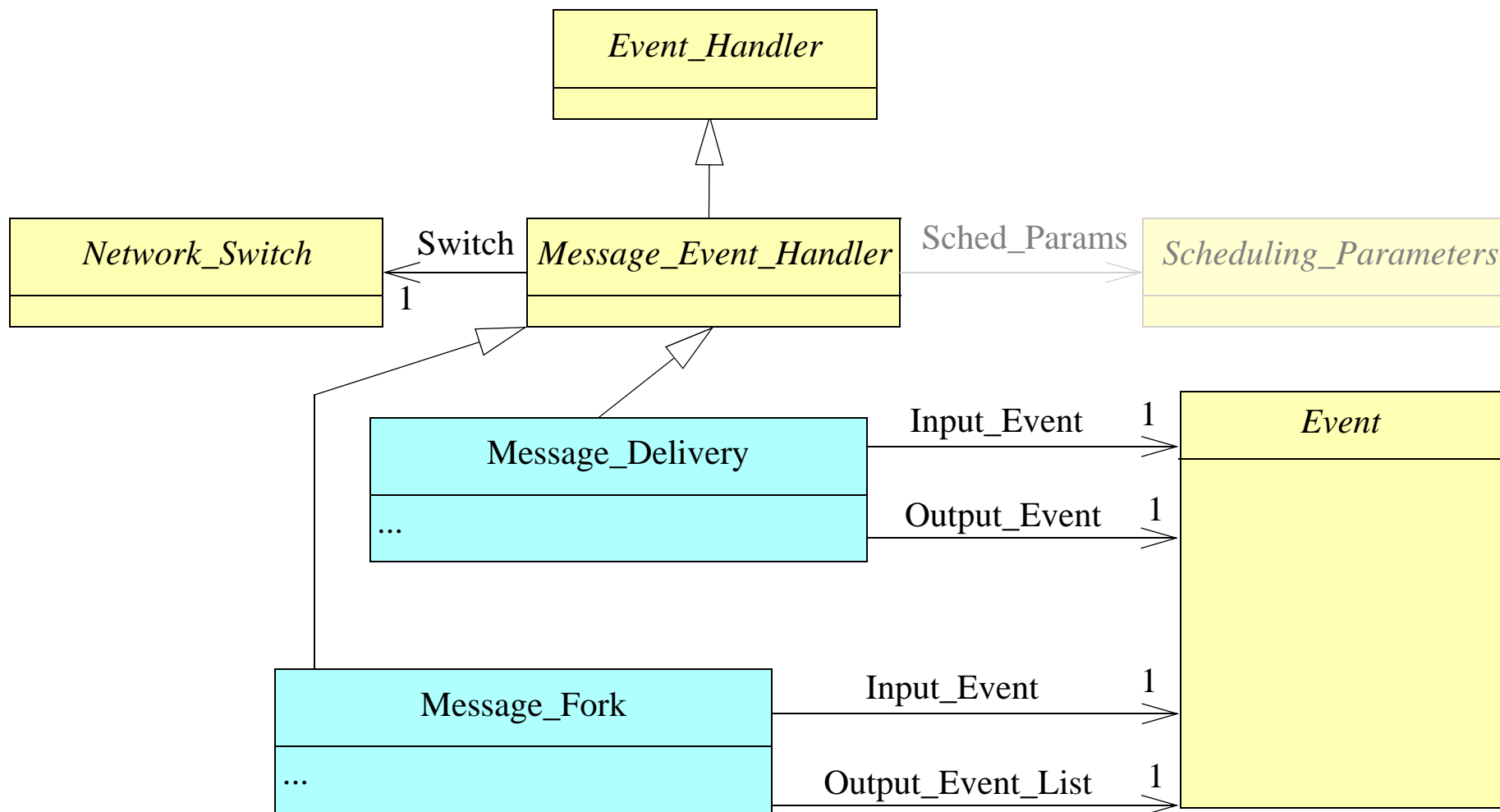
3. Networks



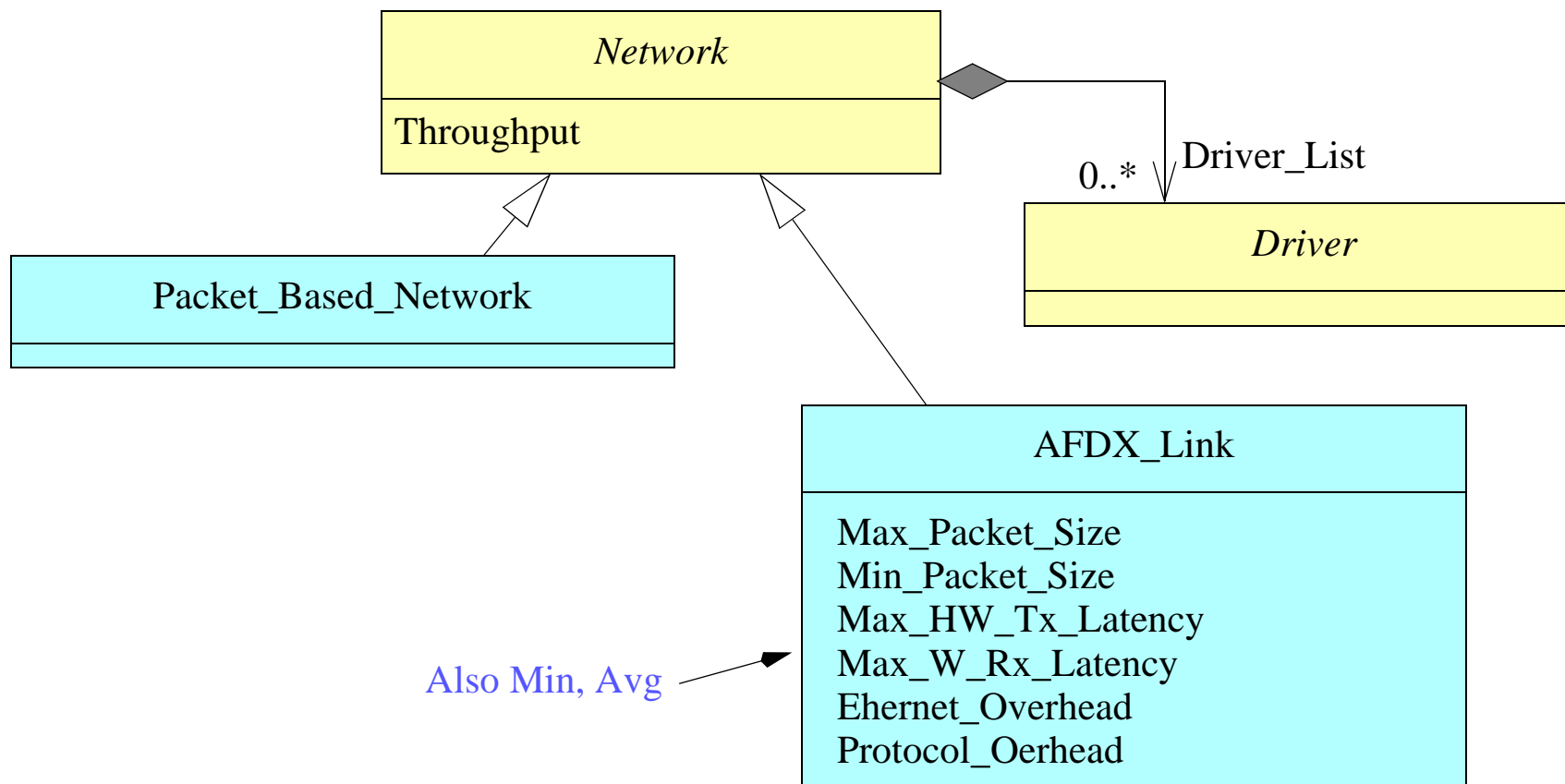
4. Network switches and routers



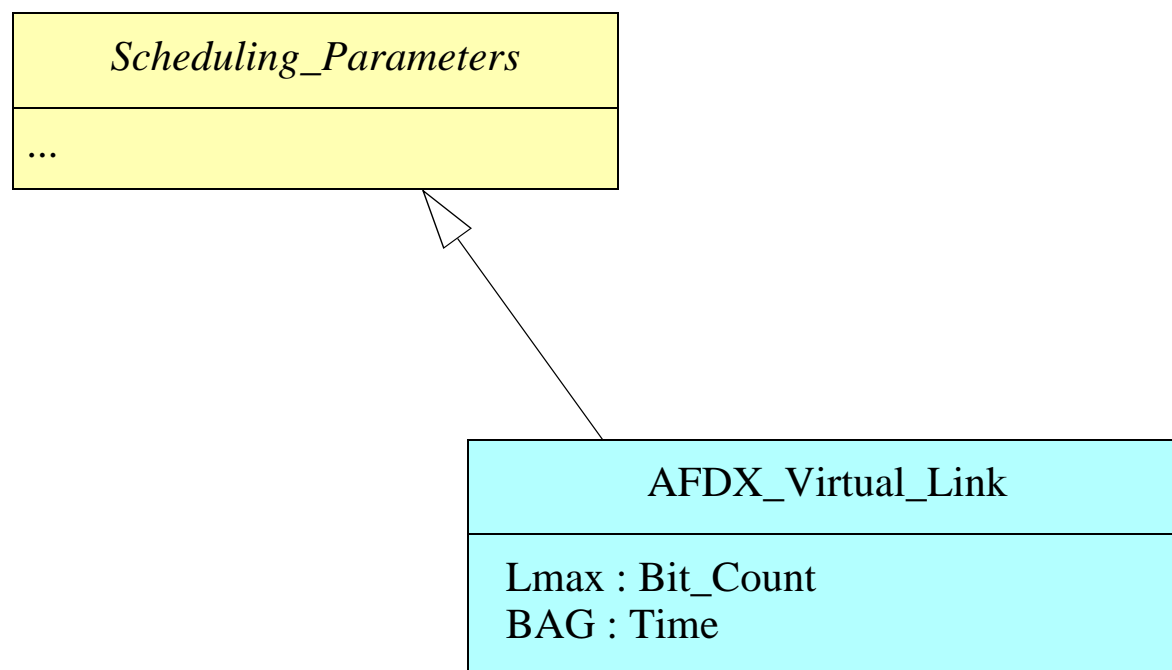
Message Delivery Event Handlers



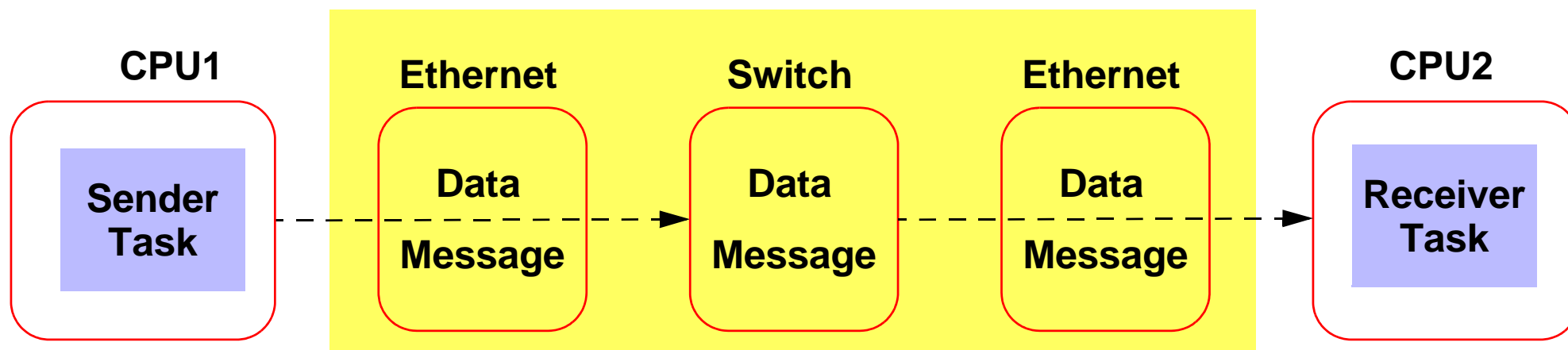
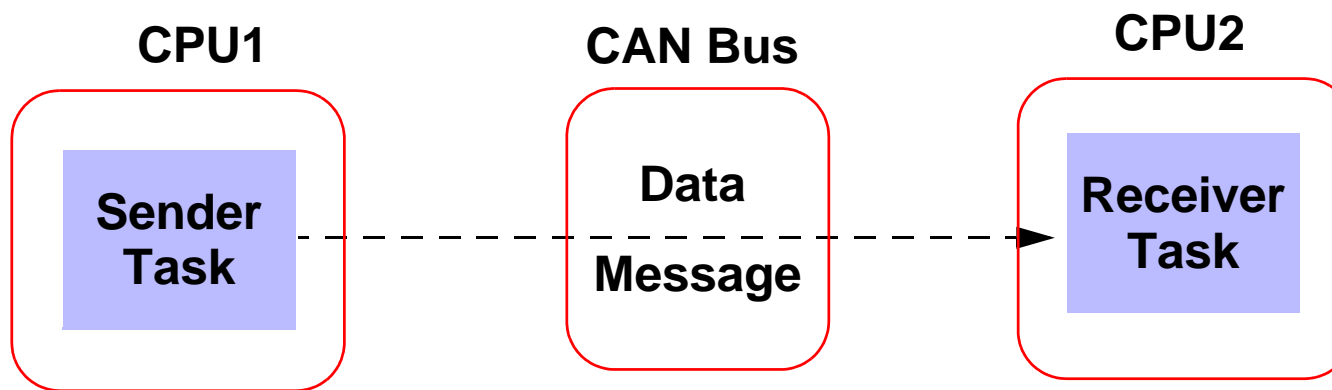
5. Modelling AFDX networks



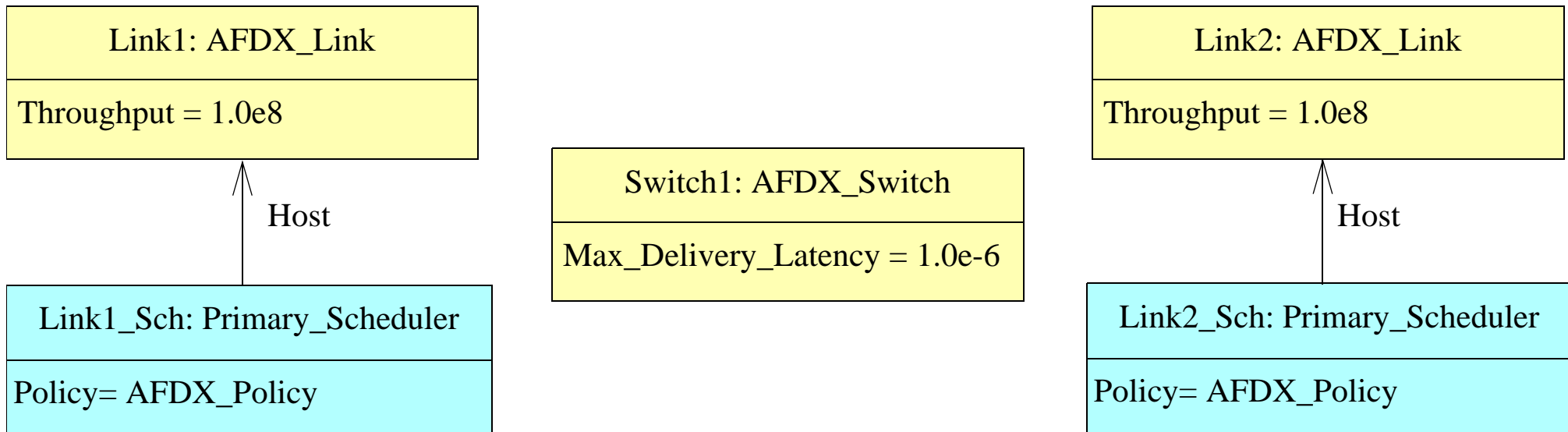
AFDX Virtual Links



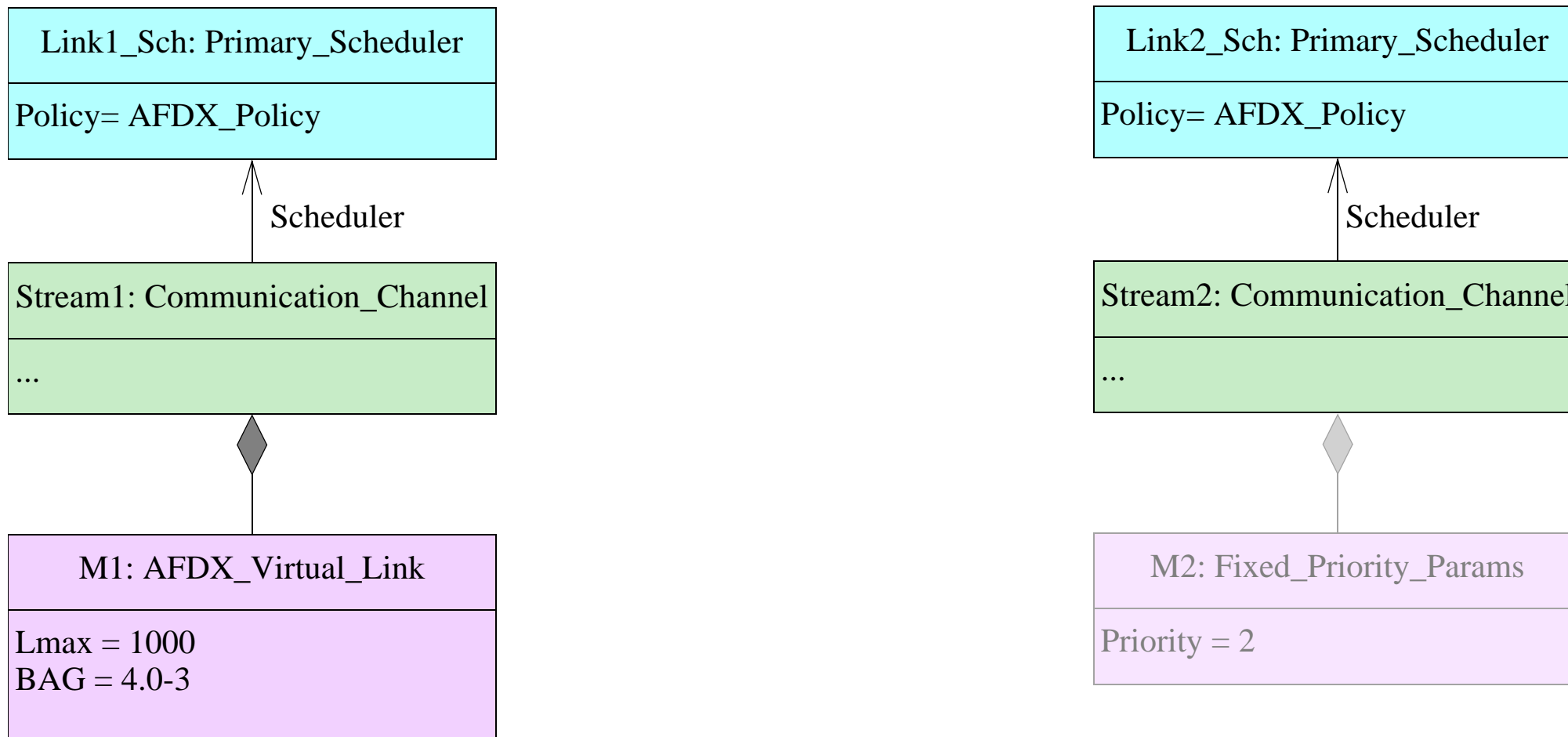
A Simple Example



Platform View



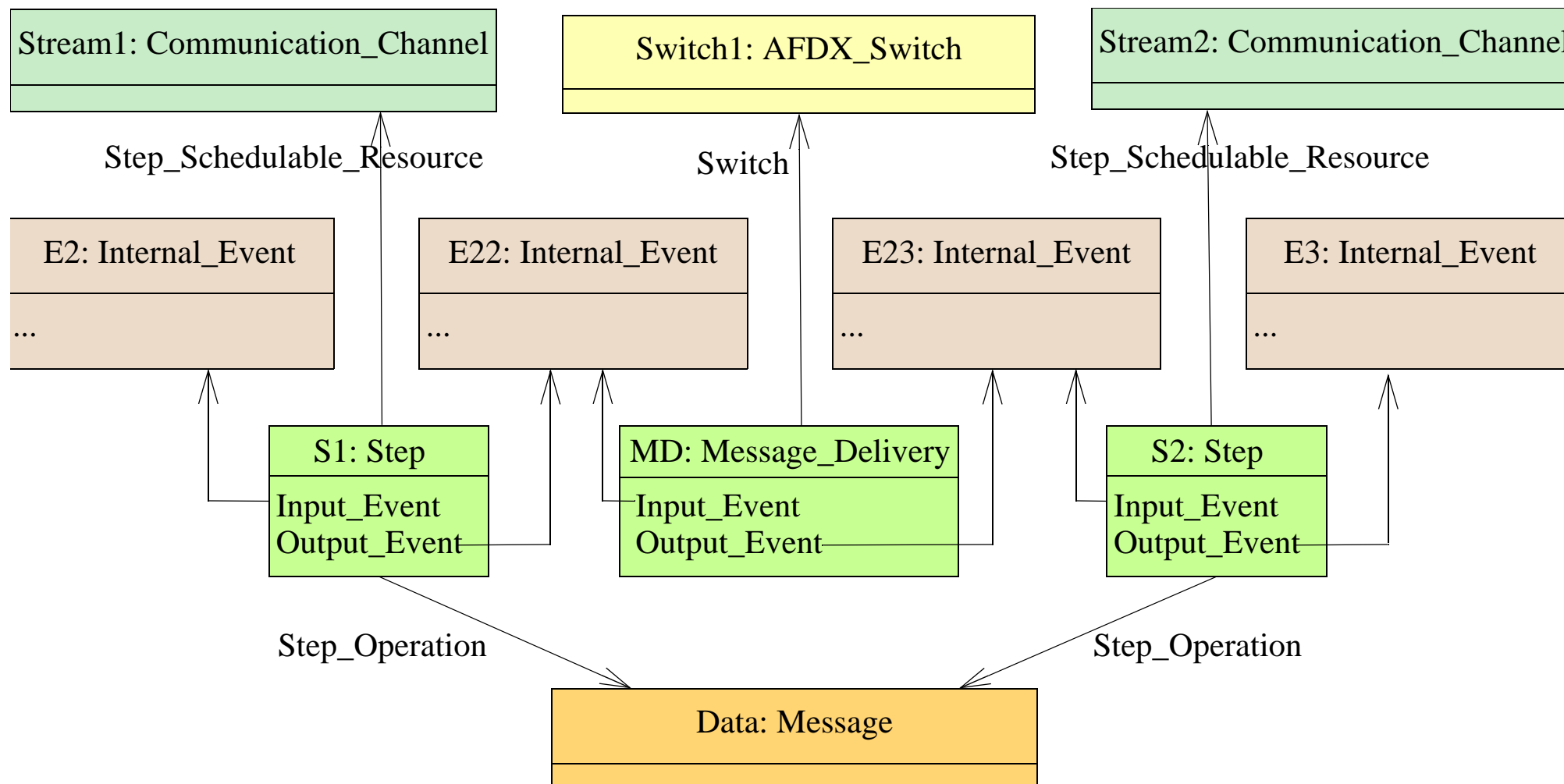
Concurrent architecture view



Operations view

Data: Message
Max_Message_Size = 1600

Real-Time Situation view

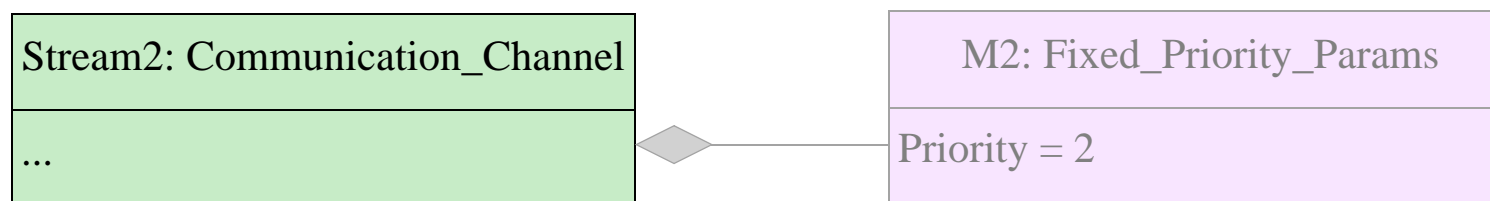


Alternatives for prioritized switch

a) Add the priority to the message event handler



b) Add the priority to the output communication channel



6. Conclusions

We have proposed new modelling elements to support

- network switches
- network routers
- AFDX real-time networks

These elements:

- are being implemented in MAST2 together with their associated analysis techniques
- will be proposed for a future version of the MARTE UML profile for real-time embedded systems