

The case for limited-preemptive scheduling in GPUs for real-time systems

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Work complementary to Amert et al.¹:

- Prior work: scheduling tasks within single context (mainly).
- This work: scheduling properties of different HW contexts.

¹Amert, T., Otternes, N., Anderson, J.H., Smith, F. D., GPU Scheduling on the NVIDIA TX2: Hidden Details Revealed, December 2017





Background: context switch mechanisms and preemption models

Experiment: Measure context switch response times

Experiment: Task scheduling on GPUs

Conclusion









Non-preemptive scheduling (current GPUs):

- Finish whole kernel.
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Limited-preemptive scheduling:

- Interrupt on work-group boundary ("SM draining"²).
- ► Max blocking: ~WCRT of work-group.
- Swap: HW+OpenCL configuration.



Our claim: SM draining, modelled by limited-preemptive scheduling, provides a good trade-off point for GPUs between:

- Context switching cost, and
- WCRT benefits.



"The Fermi pipeline is optimized to reduce the cost of an application context switch to **below 25 microseconds**."³

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- Is 25μ s an average or worst-case time?
- Is 25μ s execution time or response time?
- What is the distribution?

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Measure context switch response time - experiment

Characterise WCRT of hardware (non-preemptive) context switch.

- 1. Modify (nouveau's) context switching firmware to report WCRT.
 - **Excluding** time to finish current kernel execution.
 - Intrusive measurement, max. observed overhead 224ns.



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- 3. For several Kepler GPUs (2012-2014) gather 20M samples each.
 - 1600×1200 X.org/XFCE desktop,
 - 1024x768 OpenArena windowed timedemo.



NVIDIA	SM	Cores	Max bw	State	Т	ime (μ s	Avg. bw		
GeForce		MHz	GiB/s	KiB	Min	Avg	Max	GiB/s	Util.
GT 710	1	953	14.4	63.9	9.2	21.5	80.1	2.83	19.6%
GT 640	2	901	28.5	68.2	13.6	26.5	43.7	2.45	8.6%
GTX 650	2	1058	80.0	68.2	12.7	23.2	36.0	2.71	3.4%
GTX 780	12	992	288.4	268.6	9.7	20.0	28.6	13.76	4.8%

- What is the average context switch time? $20.0 26.5 \mu s$.
- What is the worst-case context switch time? $> 28.6\mu$ s.



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- Distribution (GT 710): 0.3% of samples in $[23.6, \infty]$.
 - see paper for plot.



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Task scheduling on GPUs - experiment

Study WCRT implications of scheduling models under context switching constraints, through overhead-aware schedulability experiment.

- 1. Determine feasible parameters/ranges for
 - · Context switch overheads for different scheduling policies,
 - (Periodic) task sets.
- 2. Compare schedulability of random task sets.



Task scheduling on GPUs - parameters

		State	e (KiB)	Time	e (μs)	Preempt				
Scheduling policy	Ctx	Reg	Local	Total	Avg	Max	/job ⁴			
Full preemptive (EDF)	68.2	512	96	676.2	263	434	×2			
SM draining (IpEDF)	68.2	0	0	68.2	27	44	×2			
Non-preemptive (npEDF)	68.2	0	0	68.2	27	44	$\times 1$			
(Based on GeForce GT 640 ($2 \times SM$), resembling Tegra K1)										

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Inflate task cost with n $\,\times\,$ context switch time

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Compare schedulability of random task sets:

Task set:

- Uniprocessor EDF scheduling policy.
- $U = \{0.2, 0.21, \dots, 1.0\}$
- ▶ 100,000*81 = 8.1M random task sets (UUniFast).
- Task set: two tasks, $1,000\mu s \leq P_i < 15,000\mu s$.
- IpEDF: max blocking $q = \frac{c}{random(2,500)}$, 2-500 WGs per SM.













For $0.25 \leqslant U \leqslant 0.72$ full-preempt beneficial

Reduce preemptive ctxswitch overhead \rightarrow higher schedulability.





Limited-preemption far outperforms other models!



Conclusion

Limited-preemptive scheduling (SM draining) provides a good trade-off point for GPUs between context switching cost and WCRT benefits.

- Current GPUs: context switch $20 26.5 \mu s$ on average.
- Overhead-aware schedulability experiment demonstrates advantage of SM draining model.



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In the paper:

- Histogram of context switch times GeForce GT 710.
- \blacktriangleright Demonstration of interference context switch \leftrightarrow scan-out.
- Schedulability experiment with 3-task systems.



NVIDIA GPU architecture - streaming multiprocessor

	Streaming Multiprocessor (SM), simplified														
Warp scheduler Warp scheduler						۷	Warp scheduler Warp scheduler						r		
Register file (65536 * 32 bits = 256KiB)															
Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
					••• ((Kepl	er: 1	92 сс	ores t	otal)					
Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core	Core
L1 + Local memory (64KiB)								Interconnect							



















