Evaluating the Memory Subsystem of a Configurable Heterogeneous MPSoC

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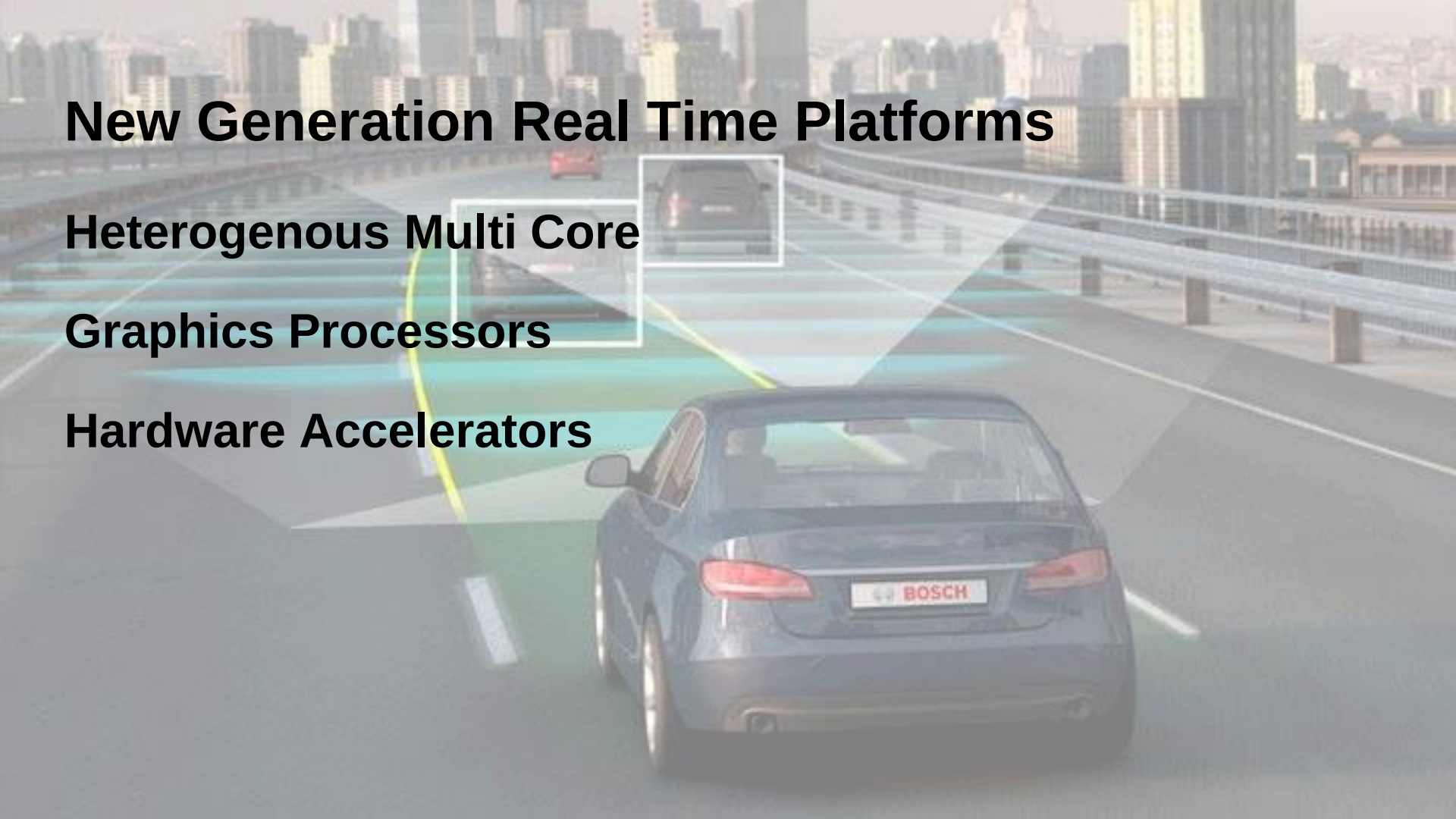
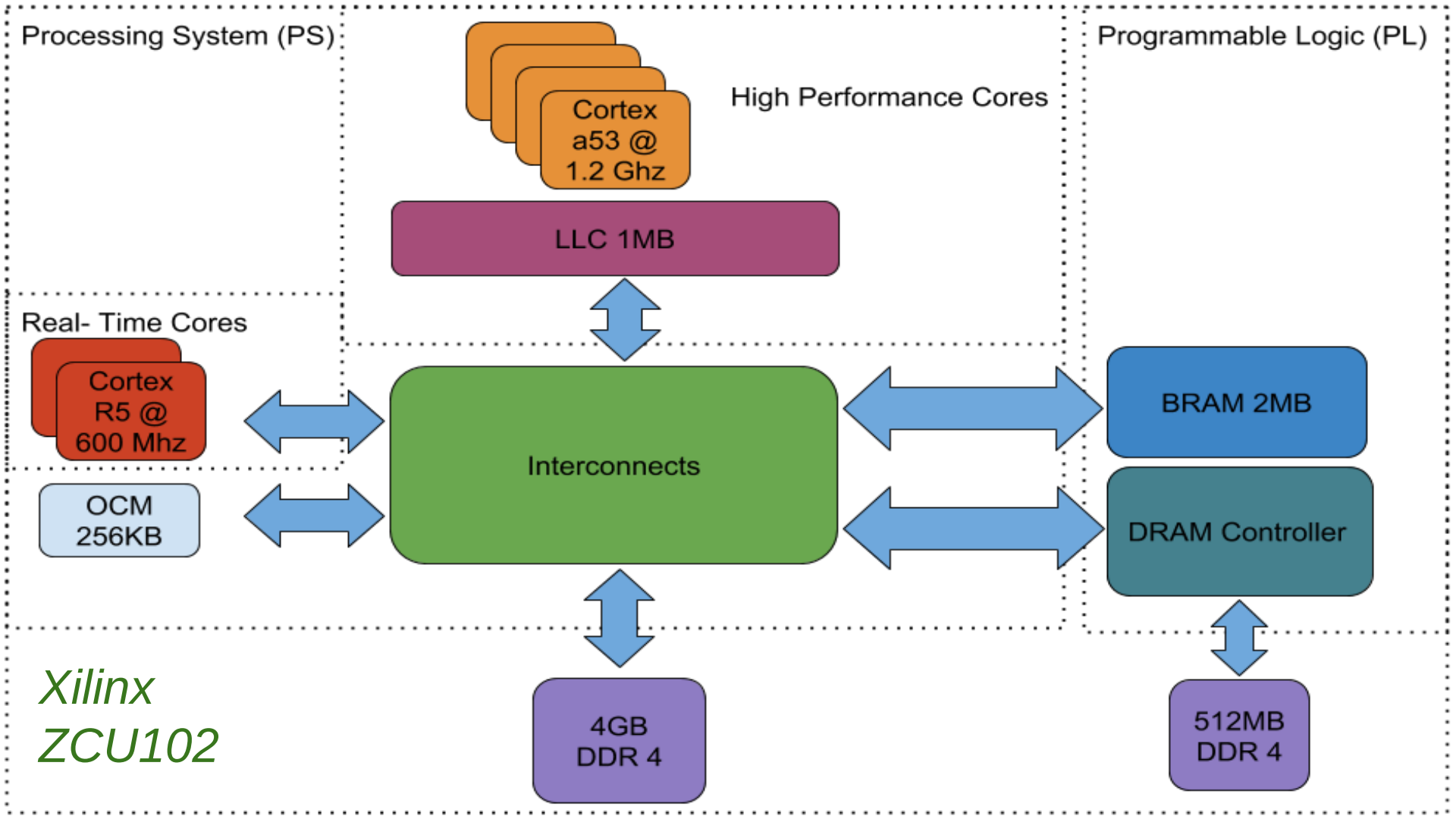


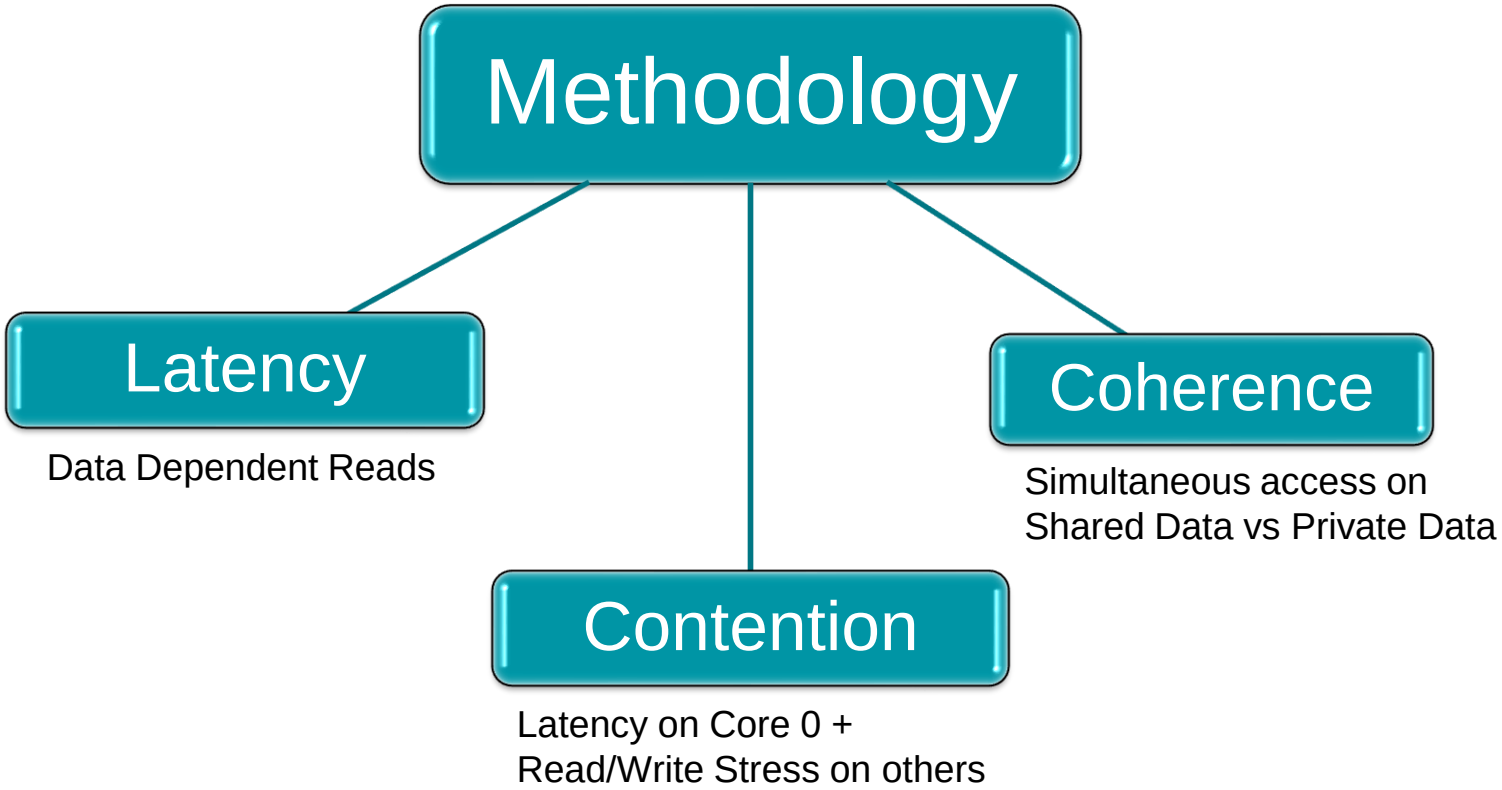
New Generation Real Time Platforms

Heterogenous Multi Core

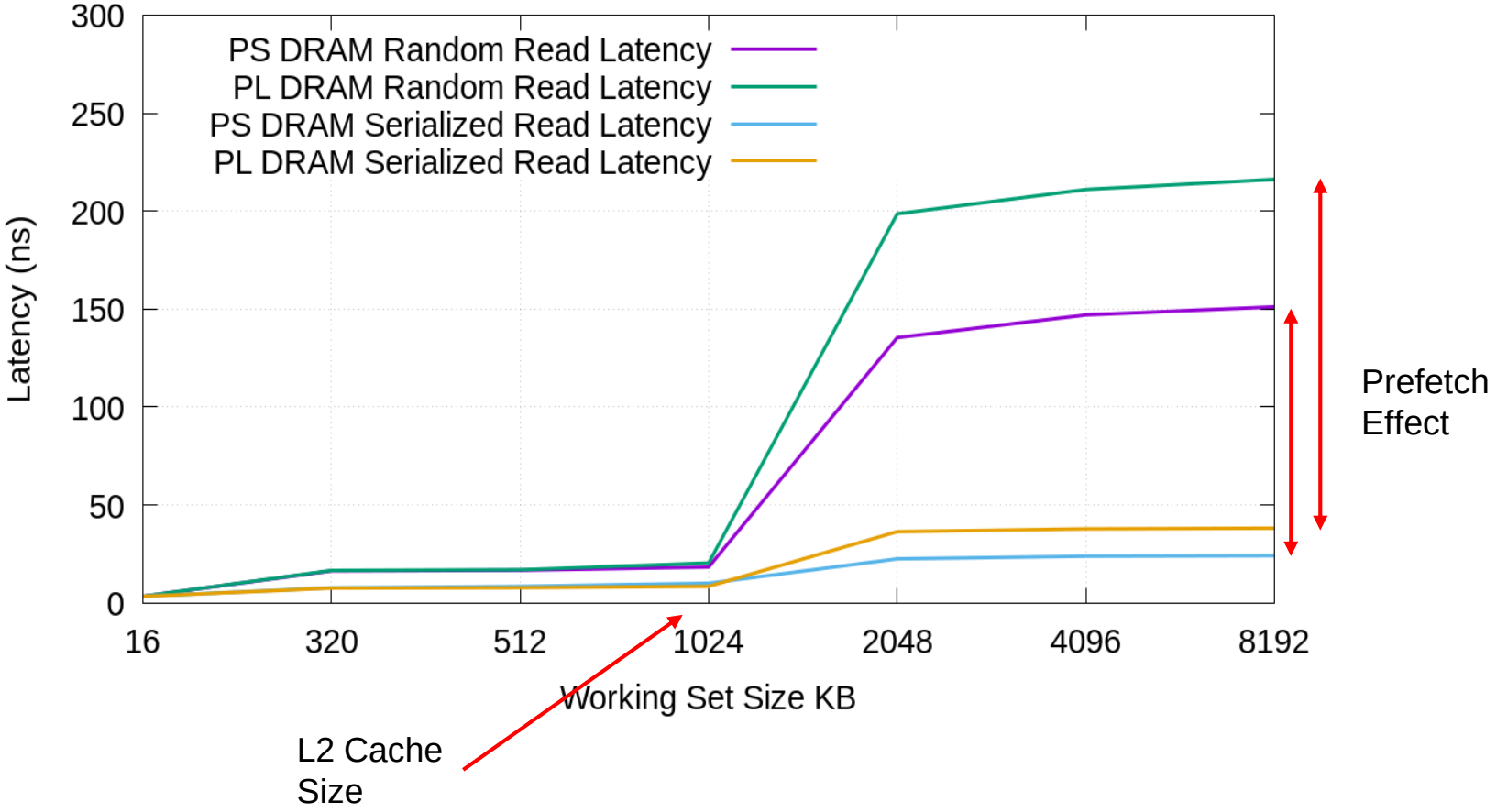
Graphics Processors

Hardware Accelerators

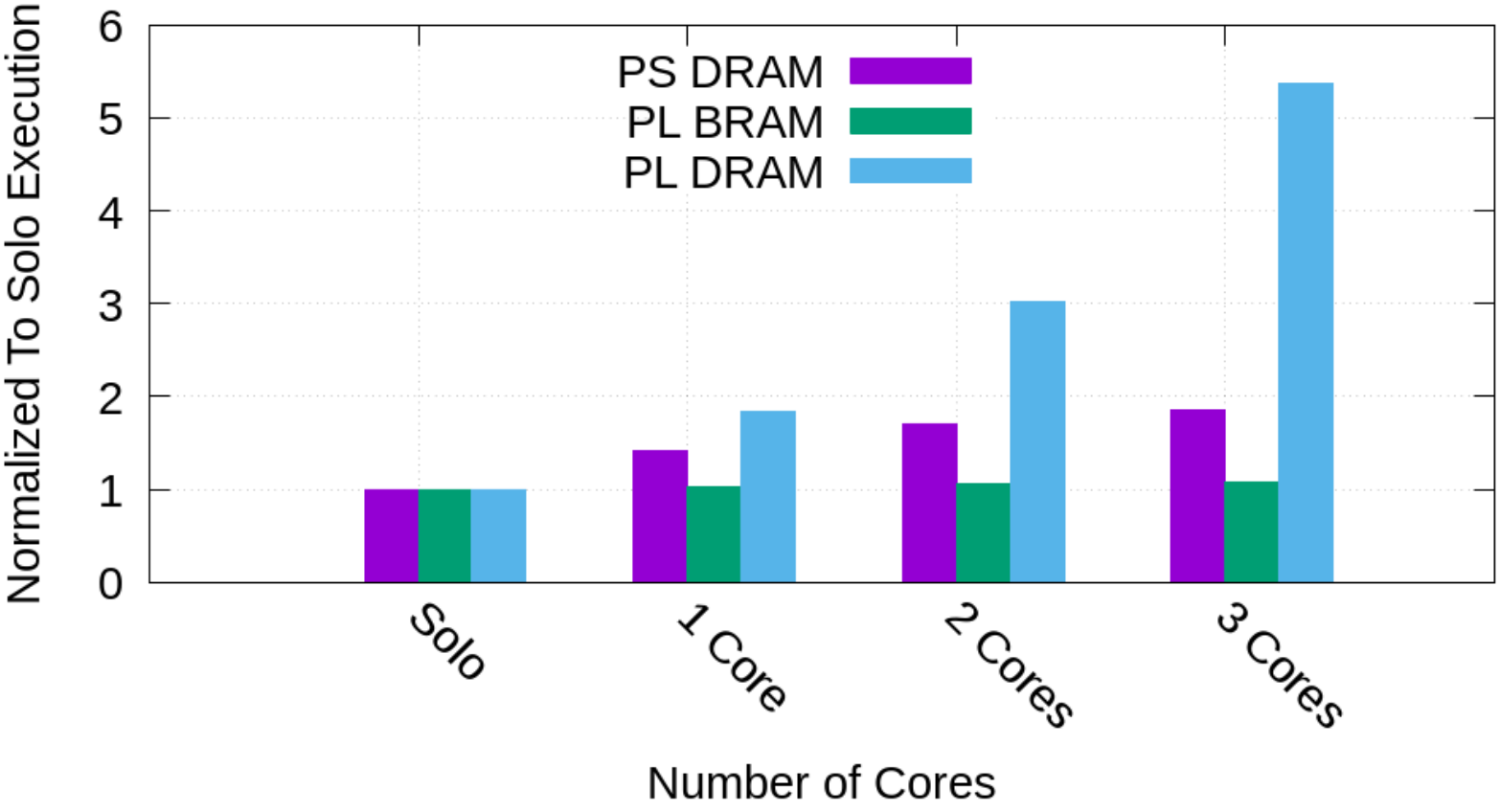

Processing System (PS)
Programmable Logic (PL)
Cortex
a53 @
1.2 Ghz
High Performance Cores
LLC 1MB
Real- Time Cores
Cortex
R5 @
600 Mhz
OCM
256KB
Interconnects
BRAM 2MB
DRAM Controller
4GB
DDR 4
512MB
DDR 4
Xilinx
ZCU102


Methodology
Latency
Data Dependent Reads
Coherence
Simultaneous access on
Shared Data vs Private Data
Contention
Latency on Core 0 +
Read/Write Stress on others

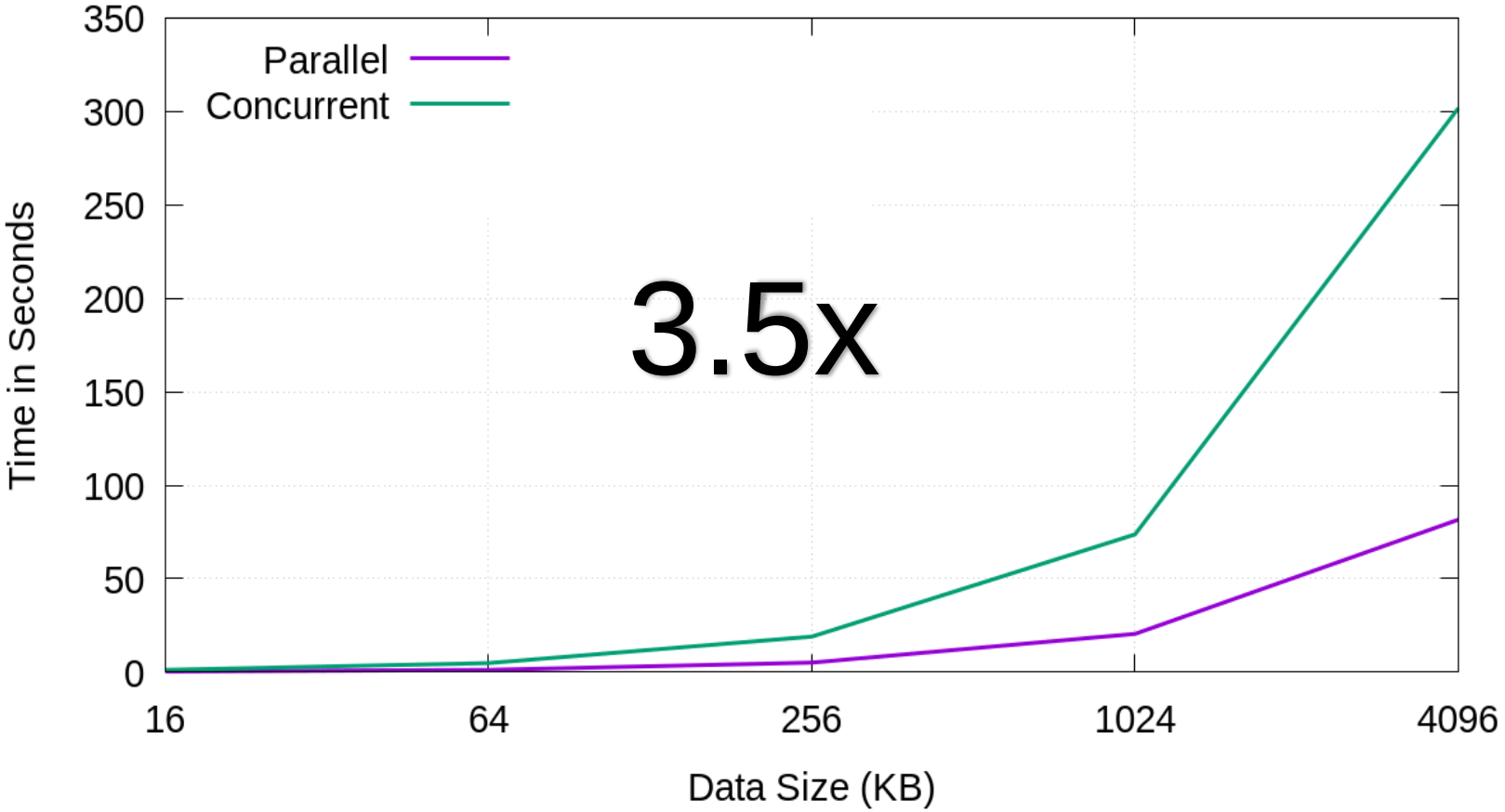
Memory Read Latency



Multi Core Contention



Cache Coherence



Conclusions

Latency: PS DRAM < PL Bock RAM < PL DRAM

PL DRAM Read Latency under Contention 5.3x increase

PL Block RAM Least affected by Contention, 1.8x

Coherence Effects 3.5x

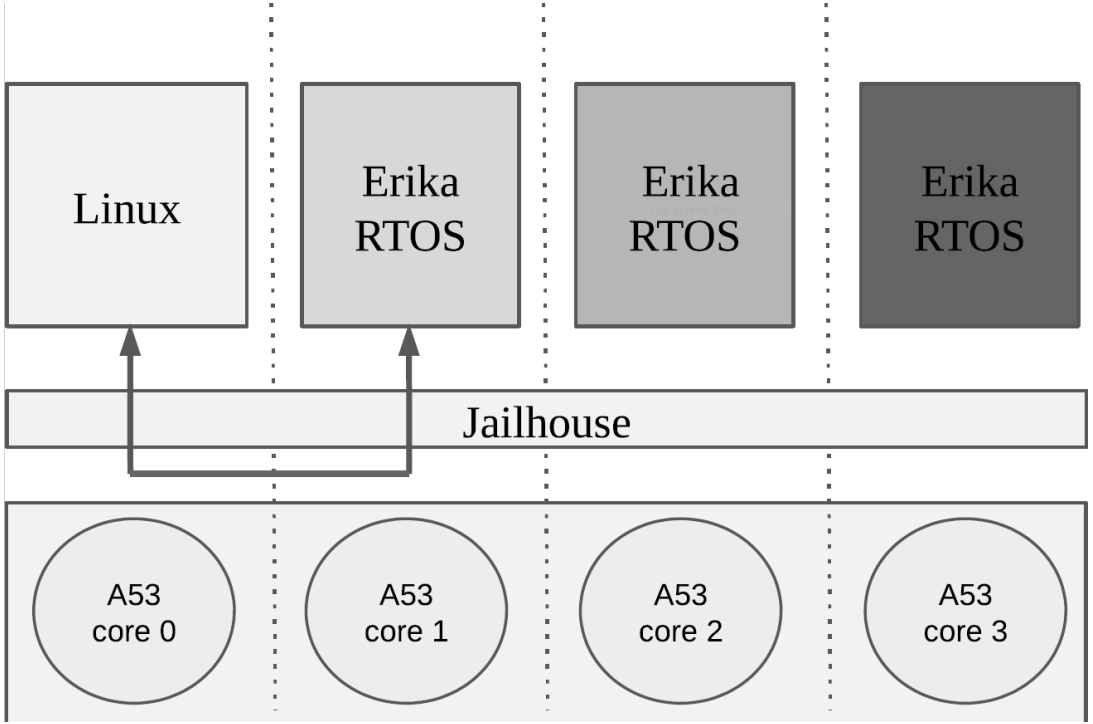
Proposed architecture

Strong isolation

Hypervisor limits shared resource access

Cache Coloring to reduce LLC contention

PL BRAM as shared scratchpad



Thank You!