Welcome to

OSPERT 2017

13th workshop on Operating Systems Platforms for Embedded Real-Time Applications

June 27, Dubrovnik, Croatia

in conjunction with

the 29th Euromicro Conference on Real-Time Systems

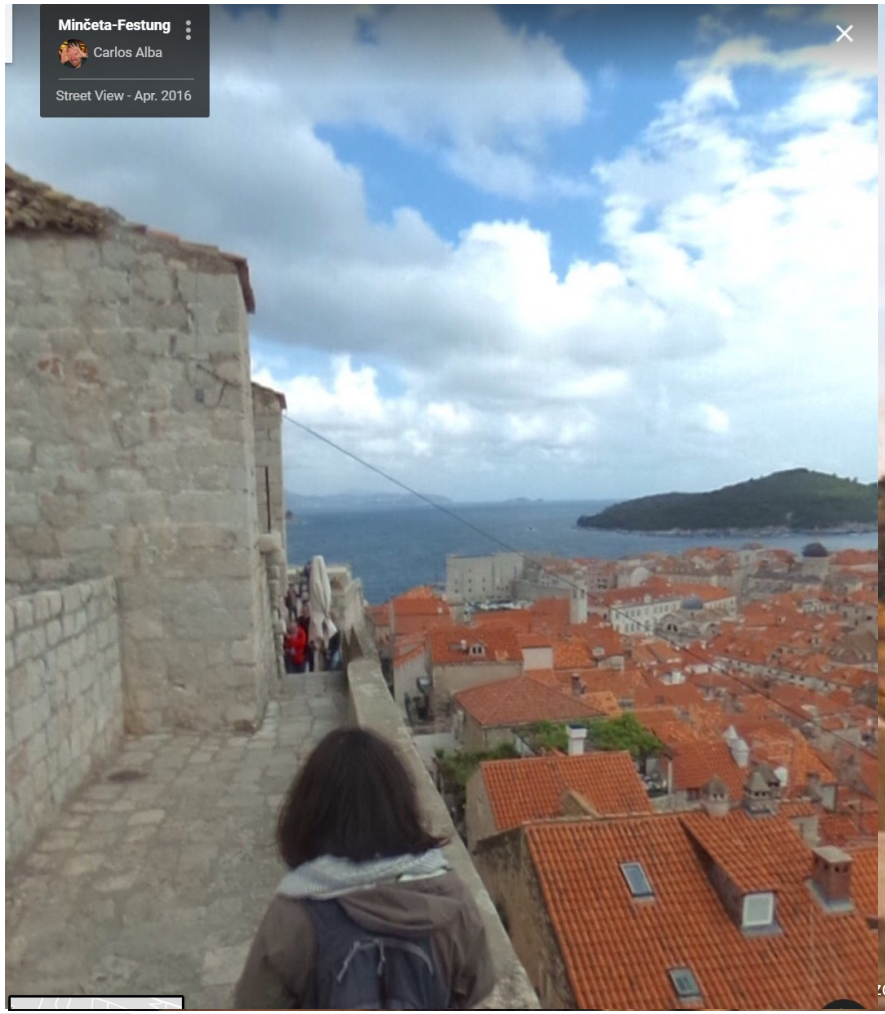
June 27-30, 2017, Dubrovnik, Croatia

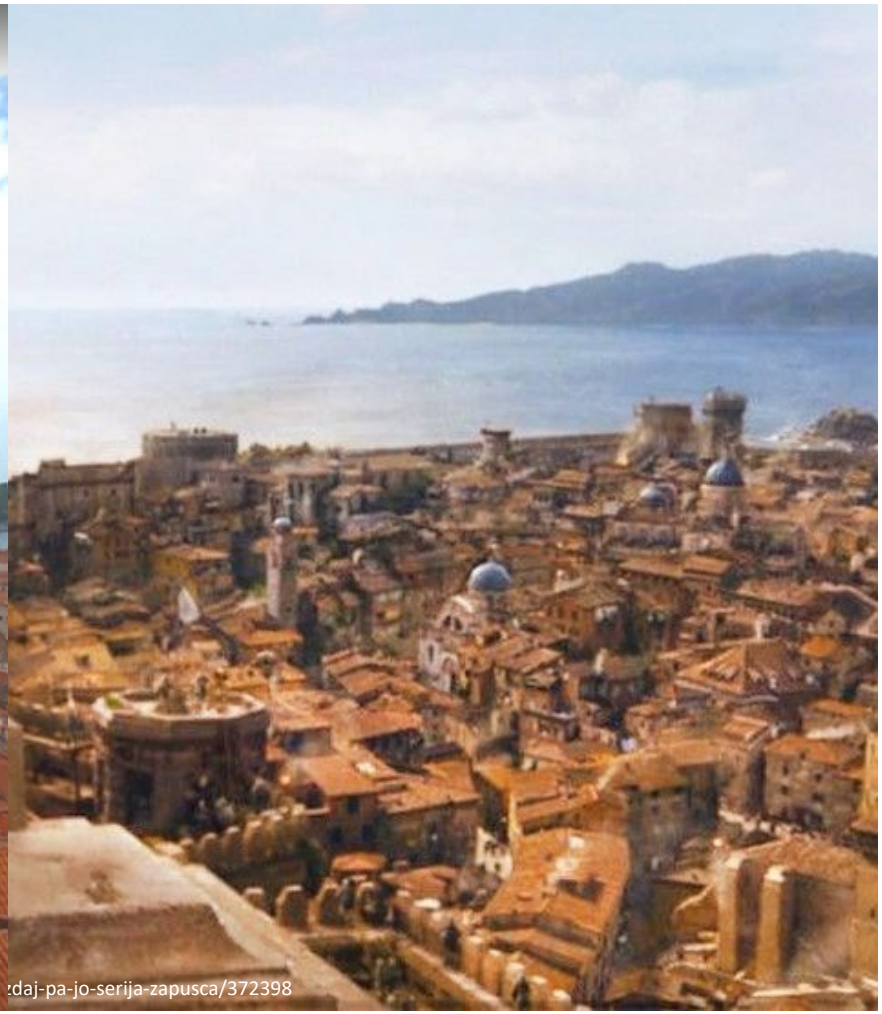
Marcus Völp, Heechul Yun

uni.lu UNIVERSITÉ DU LUXEMBOURG

KU

Welcome to Kings Landing





Numbers for the Crunchers

OSPERT 2017,

solicited diverse types of contributions, including regular and short papers as well as experimental studies.

- regular workshop papers: up to six pages
- short papers: up to three pages, intended for reports on work in progress, project status reports, and replication studies

Received 13 submissions

- 12 regular papers
- 1 short papers

Accepted 10 papers

- 9 regular papers and one short paper
- 4 independent reviews per paper

Many thanks to the program committee!

Andrea Bastoni, SYSGO AG
Reinder J. Bril, Eindhoven University of Technology
Aaron Carroll, Apple
Shinpei Kato, Nagoya University
Hyoseung Kim, University of Carolina Riverside
Juri Lelli, ARM
Guiseppe Lipari, Scuola Superiore Sant' Anna
Daniel Lohmann, Leibnitz Universität Hannover
Mitra Nasri, MPI Software Systems
Kyoung Soo Park, KAIST
Harini Ramaprasad, University of North Carolina Charlotte
Richard West, Boston University

Today's taskset

Welcome (Φ = 0, C_{marcus} = 5m)
Coffee Breaks (Φ = 1h, C = 30m, T = 5h)
Lunch (Φ = 3h, C = 1h20m)

Regular Papers (C = 25, T = 1y)
Short Paper (C = 15, T = 1y)

Sebastian Eckl, Daniel Krefft and Uwe Baumgarten
Migration of Components and Processes as means for dynamic Reconfiguration in Distributed Embedded Real-Time Operating Systems

Break (Φ = 7h25m, C = 20m)

2 Keynotes (Φ = 5m, C = 55m, T = 6h25)

- Dr. Moritz Neukirchner
  The Future of Automotive Software Infrastructure Building adaptive dependable systems
- Prof. Sergio Montenegro
  How to program space vehicles? Make it simple!

Eunji Pak, Donghyouk Lim, Young-Mok Ha and Taeho Kim
Shared Resource Partitioning in an RTOS

V

Ralf Ramsauer, Jan Kiszka, Daniel Lohmann and Wolfgang Mauerer
Look Mum, no VM Exits! (Almost)

V

Benjamin Engel and Claude-Joachim Hamann
What are you Waiting for -- Removing Blocking Time from High Priority Jobs through Hardware Transactional Memory

V

Miltos Grammatikakis, George Tsamis, Polydoros Petrakis, Angelos Mouzakitis and Marcello Coppola
Network and Memory Bandwidth Regulation in a Soft Real-Time Healthcare Application

V

Alfons Crespo, Angel Soriano, Patricia Balbastre, Javier Coronel, Daniel Gracia and Philippe Bonnot
Hypervisor Feedback Control of Mixed Critical Systems: the XtratuM Approach

V

Renata Martins Gomes, Marcel Baunach, Maja Malenko, Leandro Batista Ribeiro and Fabian Mauroner
A Co-Designed RTOS and MCU Concept for Dynamically Composed Embedded Systems

V

Nathan Otterness, Ming Yang, Tanya Amert, James Anderson and F. Donelson Smith
Inferring the Scheduling Policies of an Embedded CUDA GPU

V

Junjie Shi, Kuan-Hsun Chen, Shuai Zhao, Wen-Hung Huang, Jian-Jia Chen and Andy Wellings
Implementation and Evaluation of Multiprocessor Resource Synchronization Protocol (MrsP) on LITMUSRT

V

Adam Lackorzynski, Carsten Weinhold and Hermann Härtig **Predictable Low-Latency Interrupt Response with General-Purpose Systems**

The boring version

9:00 Welcome

9:05 Keynote: Dr. Moritz Neukirchner

The Future of Automotive Software Infrastructure
Building adaptive dependable systems

10:00 Coffee Break

10:30 The thing called RTOS

- Eunji Pak, Donghyouk Lim, Young-Mok Ha and Taeho Kim
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- Ralf Ramsauer, Jan Kiszka, Daniel Lohmann and Wolfgang Mauerer
  Look Mum, no VM Exits! (Almost)
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  What are you Waiting for -- Removing Blocking Time from High Priority Jobs through Hardware Transactional Memory
- Sebastian Eckl, Daniel Krefft and Uwe Baumgarten
  Migration of Components and Processes as means for dynamic Reconfiguration in Distributed Embedded Real-Time Operating Systems

12:00 Lunch

13:20 Memory and the other thing

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15:00 Coffee Break

15:30 Keynote: Prof. Sergio Montenegro

How to program space vehicles? Make it simple!

16:25 Break

16:45 Oh no, I got synch'ed

- Junjie Shi, Kuan-Hsun Chen, Shuai Zhao, Wen-Hung Huang, Jian-Jia Chen and Andy Wellings
  Implementation and Evaluation of Multiprocessor Resource Synchronization Protocol (MrsP) on LITMUSRT
- Adam Lackorzynski, Carsten Weinhold and Hermann Härtig **Predictable Low-Latency Interrupt Response with General-Purpose Systems**

17:45 Closing Remarks

18:15 Reception for new attendees

OSPERT 2017 Keynotes

The Future of Automotive Software Infrastructure – Building adaptive dependable systems

Dr. Moritz Neukirchner
Elektrobit Automotive GmbH

How to program space vehicles? Make it simple!

Prof. Dr. Sergio Montenegro
Aerospace Information Technology, Universität Würzburg

Session 1: The thing called RTOS

- Eunji Pak, Donghyouk Lim, Young-Mok Ha and Taeho Kim
  Shared Resource Partitioning in an RTOS
- Ralf Ramsauer, Jan Kiszka, Daniel Lohmann and Wolfgang Mauerer
  Look Mum, no VM Exits! (Almost)
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Session 2: Memory and the other thing

- Miltos Grammatikakis, George Tsamis, Polydoros Petrakis, Angelos Mouzakitis and Marcello Coppola
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Session 3: Oh no, I got synch'ed

- Junjie Shi, Kuan-Hsun Chen, Shuai Zhao, Wen-Hung Huang, Jian-Jia Chen and Andy Wellings
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Closing Remarks

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Keynote:

Moritz Neukirchner

- How does fault tolerance work with inherently imprecise image recognition and learning algorithms that may well misclassify images?
  => EB autonomous driving group looks into this
- How to ensure dependability?
  => hierarchical monitoring is critical to make the dependability case; monitor on performance system observes application and is itself checked by monitor on classical Autobest system.

Ralf Ramsauer

- How much effort it is to support different Linux versions?
  => already support 3.10 – 4.1x; little effort; all future versions once we go mainstream
- Lx features
  => virtualized Ethernet, etc., UFI
- How to partition shared resources between the Oss?
  => rely on architectural means (e.g., Intel Cache allocation technology)

Session 1:

Eunji Pak

- Actually do paging (i.e., replacing memory pages)?
  => no just manipulate virtual-to-physical translation
- How does your work compare with the SCE work?
  => It is inspired by the SCE, but the SCE was implemented on Linux, while this work is ETRI's own real-time operating system. which involves additional challenges that were not present in Linux.
- Is there contention with the TLB miss handler?
  => could be implemented lockfree, but still may access memory (e.g., the page tables) which causes TLB misses due to wrong coloring

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Session 1 (cont.)

Bejamin Engel

- Isn't there a do{…} while loop missing to retry the lock if failed?
  => more options possible than simple retry [unfortunately not discussed online]
- Transactional state cannot be migrated?
  => current work assumes uniprocessor
  [how about abort on migrate?]
- spin-/blocking impact on schedulability is known since a long time; only overheads differ when you consider HTM

Comments from chairs

Sebastian Eckl

- *Unfortunately, no questions asked so short before lunch, … [so let me pose a few here:*
- *Was the Fiasco.OC scheduling context interface sufficient to implement your migration approach? What did you have to change?*
- *Did you find migration sweet spots within the tasksets you considered? There are probably times where it is easier / less costly to take a snapshot and running from there may be worth while considering?]*

Session 2:

Miltos Grammatikakis

- Why did you not exploit the acceleration coherency port of ARMv7?
  => not really looked into video streaming; more related to arrival of video frames
- ACP allows external memory accesses while ensuring cachelines stay hot in the cache
  => not yet considered; similar draft limiter

Alfons Crespo

- How can cache-side effects from non critical partitions be mitigated?
  => use instruction threshold / time relation and decide to suspend partitions

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Session 2 (cont):

Renata Martins Gomes

- What is middleware in your context?
  => it is different; define middleware as layer bridging application and hardware
- What did you do instead of waking up the task wo. PI extension?
  => do housekeeping and wakeup next task; IRQ handler would just be set event
- Pipelined processor?
  => Vscale … [should be 5 stage pipeline]

Nathan Otterness

- How to win the arms against NVIDIA?
  => Tool set remains applicable; saw same rules on next version; create useful tool
- How consistent are the rules?
  => only early on rules were violated when we forgot to fix things; no violations right now
- Difference to WIP last year?
  => multicore scheduler uses preemption to switch between; here single context
- Context, is this something in memory?
  => Yes, it is something in memory; can't initialize Cuda Context across address spaces; didn't try mulitiple in one.

Keynote

Sergio Montenegro

- Which hardware redundancy features in the OS
  => adapt to available redundancy (given as constraint); 3-5 sometimes 6 CPUs which are able to communicate; can't turn all processors off at once; at least 2 remain and all know envelope of known good behavior; wrong decisions don't cause immediate crash (reboot in short time)
- dead code => required to make static checker happy (can be stupid)
  => Prover may be able to remove this check; how to verify robust system
- Did you experience attacks
  => need a big antenna; none seen, yet; we don't even use authentication

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Session 3:

Kuan-Hsun Chen

- PID elimination is a dirty hack
  => YES!
- Comparisson against spin based protocols would be more fair?
  => work originated from PPCP; acknowledge slightly unfair, but wanted to make the point that you should take care of unexpected behavior

LinuxRT Status

- Thomas Kleixner: double digit microseconds latency
  => not Lx RT; nice parts are still not merged
  Lot of peripheral; core stuff are not; rewrite CPU hotplug

Adam Lackorzynski

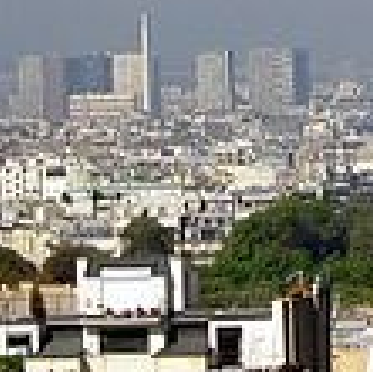
- Linux program with a bit of L4 in it
  => Linux does not intercept L4 systemcalls
- What if app calls Linux Syscall
  => go back to LX; in VM cannot block outside operating system; here block outside on L4 side
- Interrupts, Scheduling, … handled by linux
  => no, not scheduled by Lx; run in uninterrupted mode; can signal decoupled app
- Paravirt.; device goes through HV -> LX -> App; difference to Quest V
  => with Interrupt passthrough you can directly post into linux; not yet there, but this is not the source of jitter; decoupling removes LX jitter
- Evaluation: measure interrupt from device (timer); measured complicated device;
  => device is not important; real device would need strobe to measure

RTSS '17 Workshops Advertisement

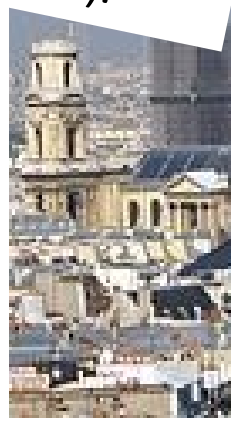
Bring together real-time, securit
distributed systems and fault
tolerance experts …
to answer questions like the o
Jim has asked this morning

CERTS

on real-time systems that
fe while under attack (in
on the timing plane).



Antonio Casimiro	University of Lisboa	
Marcus Völp	SnT - University of Luxembourg	
Sibin Mohan	University of Illinois	
Marisol Garcia-Valls	Universidad Carlos III de Madrid	
Important Dates:	Submission Deadline	mid Sept.
	Workshop	Dec. 5



see you in Paris

Really the last things

Many thanks to the authors and the PC for an interesting day!

OSPERT'18 deadline likely end of April, 2018.
Submit early, resubmit often!

Consider submitting replication studies or other experimental studies.
Get early feedback on your RTAS submissions.

Feedback and suggestions for next year?

18:30 First comer reception
(red dots meet blue dots)